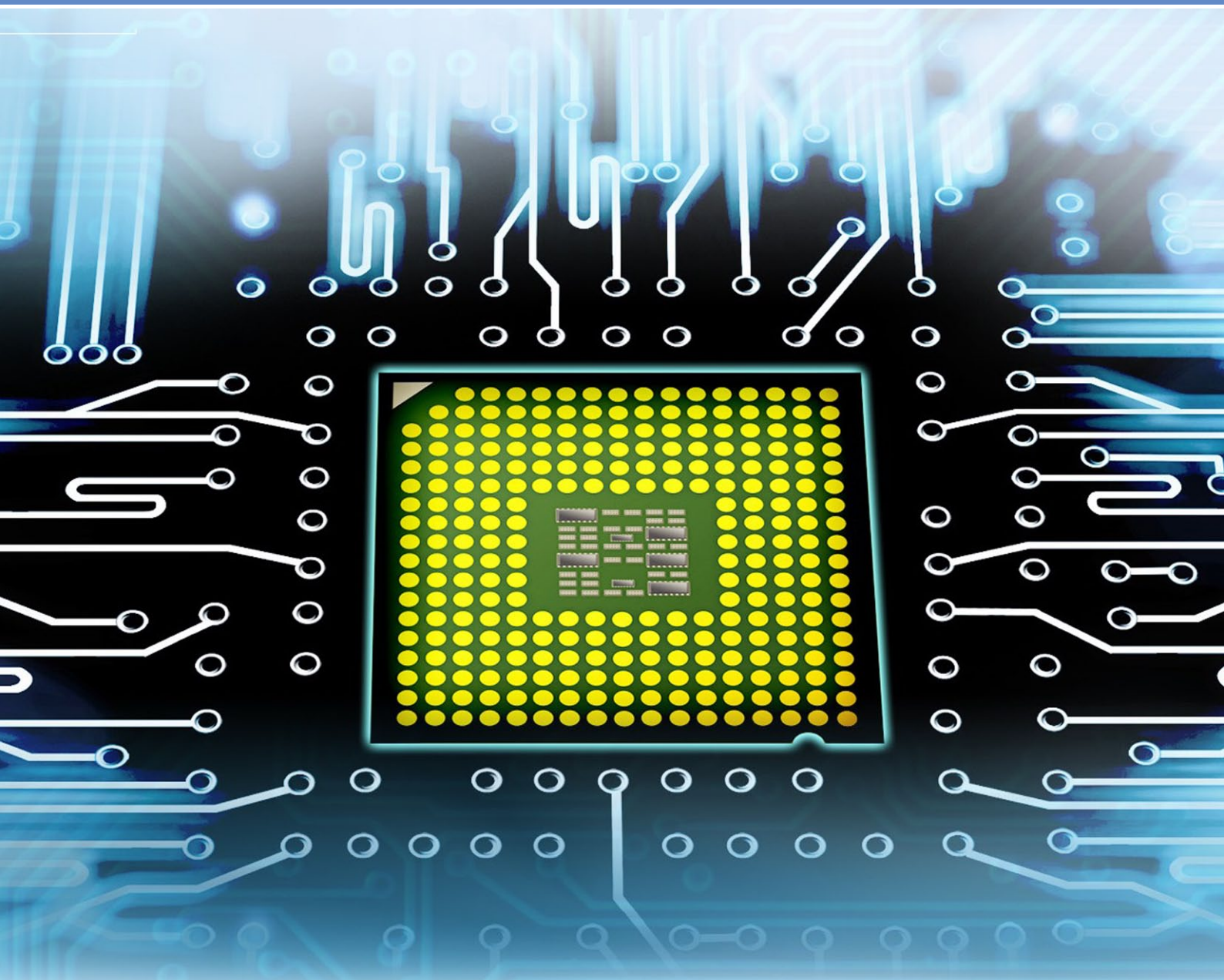


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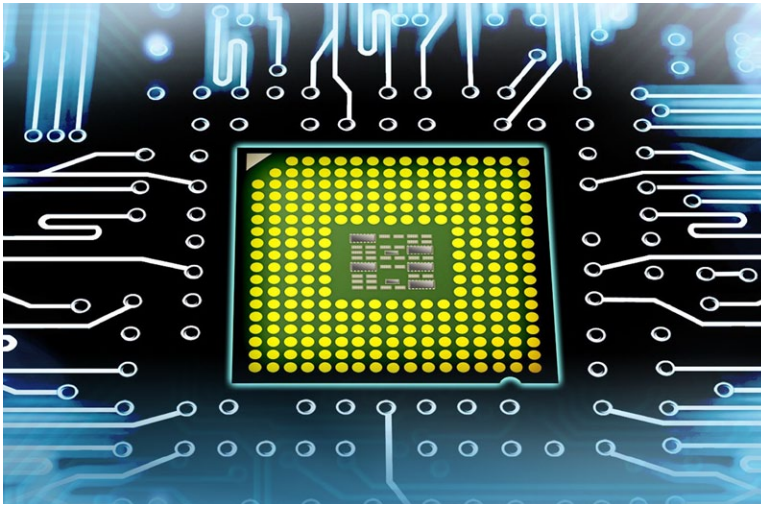
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Cover image; Drivers for optical nets at 100G rates

Texas Instruments created this graphic to illustrate its transimpedance amplifier designed to drive 28 Gbps signals for 100G optical nets. TI's first transimpedance amplifier (TIA) for the 100G optical networking market, the four-channel device supports high performance in optical networking systems at 28 Gbps for aggregate 100G data rates. ONET2804T, TI says, offers high levels of sensitivity with negligible cross-talk penalty and low input-referred noise (IRN) to provide stable and robust communication in hot-pluggable transceivers. The newest member of TI's broad optical networking portfolio, the 100G TIA serves parallel optical interconnects in applications with data rates of up to 28 Gbps, such as optical line cards, point-to-point microwave backhauls and video over fibre. Read the complete item [here](#): TI offers background on the technology challenges of 100G networking; [how to address 100G growing pains](#).

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CHRONOMETER OR CONNECTED COMPANION?

What to make of the Apple Watch? I should say, as I have done previously, that I'm not an Apple "fan". That is, I appreciate the attention to product design, production engineering and user interfaces, and to brand values, that the company's products (mostly) exemplify, but I'm not first in any queues, or indeed in the queue at all, to acquire any particular Apple product. I am reliably informed by those who are of that persuasion, however, that the Watch meets the criteria, ticks all the boxes, of "I've seen it / I must have it as soon as possible" that those smitten with the brand habitually apply. So be it.

In passing, and with the iPhone 6 release, a report from analysts IHS finds that Apple has lost none of its flair for asking (and getting) premium margins on selling price for features that cost it modest sums to add to the bill-of-materials; IHS determined that that ratio, for the step from the iPhone 6 to the 6 Plus, was close to a factor of 10.

Several things about the Watch were predictable; it's a companion to, and a 'satellite' of, an iPhone and doesn't do much without one; it gathers a certain amount of biometric data from the wristband; and so on. There are classic Apple user-interface touches such as the use of a traditional-looking watch crown to scroll through pages. What was less obvious is that Apple has grasped that a watch is a personal item in a way the phone is not (unless you habitually dress your phone in outlandish skins, I guess). So there are very many variations in case size, colour and material; even a gold case, and with a proper sapphire crystal - it being impossible to protect a watch glass from robust everyday contact with any number of surfaces.

So the design makes more than a passing acknowledgement of the fact that a watch - whatever connected-device-stuff it does - is principally an item of jewellery. I understand that Apple preserves its individuality in branding above all else - nevertheless, I am faintly surprised that the company didn't look for some co-branding with one of the big names in the luxury watch business. Not to mention any names, but thinking of the category of makers whose products cease to be a "watch" and become a "chronometer".

As it happens, we can mention one name in the fashion watch sector, as it's public that a tie-up exists between Intel and Fossil - so that thread for possible product development is out there.

If it were my place to worry over the market prospects for the Apple Watch, or indeed any connected watch product - once the new-product euphoria has worn off - what might give me sleepless nights would be this; I would not be concerned about ill-tempered sniping from the sidelines, that it doesn't have this or that function or app, or that it doesn't (yet) do all the things that the pre-launch hype suggested it might. Just throwing more development effort, technology, and software at the problem will get over that.

I might not even fret over the fact that in the watch (as timepiece, or as jewellery) we have a concept that has come to be something which needs no attention for years at a time: rather than something that's barely going to get through a day without a charge. Free-space charging while-you-walk-about, as proposed by companies such as Energous and Witricity? I'd be surprised if someone in the Apple lab isn't deep into that concept. My nagging worry would be the fact that a large proportion of my target demographic no longer wears a watch at all; when it has become second nature to check your smartphone every few minutes (no, I don't, either, but 'most everyone else seems to, these days) then the wrist-borne timekeeping function has been effectively replaced. Will added functionality breathe new life into wearing an object on your wrist, or has a tipping point been passed? Have I (I might wonder, in my imagined role) spent a large amount of research effort and budget on a product whose basic usage model is already history?

Even if that were to be the case, there's more than enough business to be had in smart watches to make some money for Samsung, Apple and the rest, for now. My guess would be that picking up the watch paradigm will, before too long, turn out to be just one step on the route to giving us a wearable terminal for our "connectedness" that is more subtle - more intimate, even - than can be packed into the wrist-worn format.

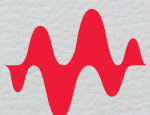
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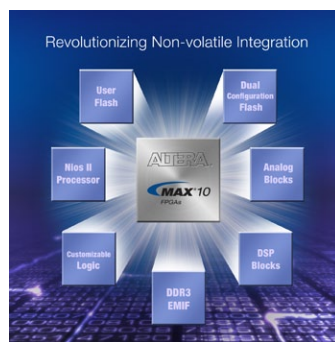
pulse

Altera's MAX 10 FPGAs blend programmable logic and analogue

Altera has formally introduced its MAX 10 FPGAs, that it previewed in May 2014; they are Altera's latest addition to its Generation 10 family. MAX 10 FPGAs host up to 50k logic elements, plus programmable analogue blocks, and retain their configuration in dual-configuration flash memory. By use of a soft-core Nios processor, they can also host embedded processing. Using TSMC's 55 nm embedded flash process technology, they are non-volatile FPGAs with dual-configuration flash, DSP, analogue and embedded processing capabilities in a small-form-factor, low-cost, instant-on programmable logic device. First chips in the family are available now together with support in a Quartus II software update, evaluation kits, design examples, documentation, training and design services. The products bridge the CPLD and FPGA market sectors, Altera says.

The flash memory is large enough for two complete configuration files, that are loaded into SRAM – the logic is conventional SRAM-based FPGA from Altera's other ranges – at power-up or on command, in around 10 msec. You can use the twin configurations for alternative functionality, for secure field update or to hold a back-up function set. Altera says it decided not to place a hard processor core on the chips, using instead its Nios II soft core, which is itself configurable to use under 5k logic elements (LEs) down to as few as 800 LEs; the device family

spans 2k to 50k LE capacity. Nios II is "more than adequate" for the processing power required by the type of designs that Altera



envisages for the devices, the company says. Analogue blocks include ADCs and temperature sensing diodes, and up to 18-channel multiplexing. The integrated analogue functionality allows MAX 10 FPGAs to be used in applications that require system monitoring, such as temperature control and touch-panel human-machine interface control. Integrated analogue blocks reduce board complexity, lower latency and deliver more flexible sample-sequencing, including 2-channel simultaneous sampling.

The device's integrated functions combined with small package options (as small as 3 x 3 mm) make MAX 10 FPGAs an effective solution for space-constrained systems, such as automotive and industrial applications. In advanced communications, compute and storage applications, MAX 10 FPGAs can efficiently manage complex control functions, while performing system configuration, interface bridging, power sequencing and I/O expansion.

MAX 10 FPGAs are available in commercial, industrial and automotive (AEC-Q100) temperature grades. There are evaluation kits, downloadable design examples, and free MAX 10 FPGA development software. Evaluation kits start at \$30, and the smallest (2k LE) chips will be around \$1.50 in volume.



USB-powered, PC-based, mixed-signal scopes with ARB

The PicoScope 3000D Series mixed-signal oscilloscopes (MSOs) are USB-connected devices that form a complete portable test system, with two or four analogue channels and sixteen digital channels as well as a built-in arbitrary waveform generator. An upgrade to the prior 3000 series, key specifications – sampling rate, buffer size and display update rate – have all been improved, while the units remain USB-powered.

The PicoScope 3000D Series MSOs are available with analogue bandwidths from 60 MHz to 200 MHz. Maximum digital input frequency is 100 MHz, equivalent to a data rate of 200 Mb/sec (5 nsec pulse width) on each channel. All models come with a USB 3.0 interface and are fully compatible with USB 2.0, giving high performance and fast update rates with both port types. The deep memory buffers of 128 to 512 megasamples,



much larger – Pico says – than other scopes costing several times more, allow long captures at fast real-time sampling rates of up to 1 Giga-sample per second. Hardware-accelerated data processing maintains smooth and rapid display updates even with very large capture sizes. Features include math channels,

automatic measurements with statistics, spectrum analysis and colour persistence display mode. Also built in are advanced digital triggering with pulse width, window, dropout, channel logic, digital pattern and other qualifiers, mask limit testing and alarms. Serial decoding supports SPI, I²C, I²S, RS-232/UART, CAN, LIN and FlexRay protocols on up to 20 analogue and digital channels, even with a

mixture of protocols at the same time.



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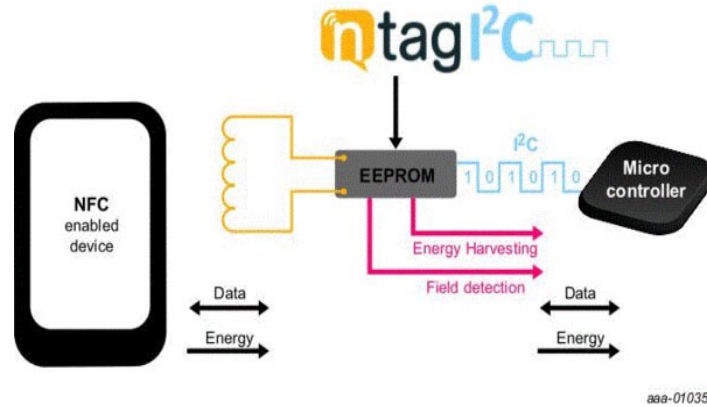
NFC + I²C combo; a passive solution for NFC interaction

NXP's NTAG I²C solution enables feature-rich options on home appliances and wearable devices – as well as the ability to power itself. The NTAG's I²C memory can be accessed via the existing embedded microcontroller of any electronic device. By combining a contactless NFC interface with a contact I²C interface and onboard non-volatile memory, the NTAG I²C solution enables – NXP says – new kinds of NFC tag interactions, including advanced device pairing, personalisation of electronic devices, and device maintenance. While existing NTAG solutions can only interact with NFC-enabled devices, the new NTAG I²C memory can be accessed via the existing embedded microcontroller of any electronic device.

Intended for very low-power operation, the passive NTAG I²C solution is capable of energy harvesting from the mobile device to power external circuitry such as low power MCUs. It also includes a field-detect function for automatic power-up, so that the mobile device's battery is not drained during standby while waiting for a NFC phone. As the first fully ISO 14443A / NFC Forum Compliant Type 2 Tag chip with I²C interface and energy harvesting with on board EEPROM, the NTAG I²C solution ensures compatibility with all NFC-enabled devices and allows data to be saved even if the power supply is lost. These features combined suit the NTAG I²C for the configuration, calibration

or customisation of wearable devices.

The NTAG I²C features a specific pass-through mode, which allows the device to serve as a communication pipe for unlimited bi-directional data exchange between the feature-rich NFC device, which may have a connection to the cloud and an advanced user-interface/display, and the electronic devices. The new device is also supported by the MIFARE SDK (Software Development Kit). Designed to provide access to all hardware features on Java level, the MIFARE SDK streamlines the development of Android apps to interact with NTAG devices. The SDK allows Android app developers to concentrate efforts on designing creative apps for a wide range of new applications that support the Internet of



Things (IoT) and wearable technology.

“The NTAG I²C [takes] NFC beyond its traditional ecosystem consumers [can] use their existing NFC-enabled mobile phones as a remote user interface, rather than relying on expensive touchscreens or Wi-Fi connectivity for wireless data exchange on home electronics,” said Rutger Vrijen, vice president and general manager, tagging and infrastructure business line, NXP Semiconductors.



Inverter design for brushless AC motor control

RX111 motor control kits are inverter reference solution kits designed to drive any 3-phase permanent magnet synchronous motors (PMSM), also called brushless AC motors. The RX111 inverter kits eliminate the need to tune their motor parameters and evaluate the best tuning algorithm coefficients. RX111 inverter kits, says Renesas, revolutionise the integration of 3-phase motors in equipment. Based on Renesas' 32-bit RX family of MCUs running at 3V, they deliver 50 DMIPS at 32 MHz. The RX111 reference kits are designed for equipment requiring medium and high dynamics and a low-cost bill of materials. The kits provide up to 7 A(max) at 24 VDC and have been tested with more than 30 different motors. An external power stage is available that is fully-compatible with the existing RX220 and RX62T inverter kits. The new RX111 solution kits provide the dynamics required to drive motors with

a high level of accuracy. The inverter kits provide:



few clicks. The solution kits also feature a sensorless vector control algorithm, which is used to accurately control the speed and the torque.

- Auto-tuning of the current proportional-integral (PI) coefficients: Kp, Ki
 - Identification of intrinsic motor parameters: Rs, Ls, Lm
 - Real-time visualisation of the motor phase, current and step response
 - Dynamic modification of the PWM frequency and control loop
- The kits include an intuitive PC graphical user interface (GUI), providing engineers with a ready-to-use inverter reference prototype that enables them to drive their own motors in a



Turning off the tick in the RTOS cuts MCU power

Segger has added tickless low power support to its embOS real time operating system. The tickless low power feature reduces the power consumption for battery powered devices; it stops the periodic system tick interrupt during idle periods. Instead of having a timer interrupt for each system tick the timer is reprogrammed to be able to spend as much time as possible in low power mode. One of the most common ways to reduce power consumption is to keep the processor in sleep (idle) mode for as long as possible. Typically an RTOS will wake the processor on a regular system tick - even if there is nothing to do. The embOS tickless low power sup-



port reduces power consumption by creating a variable length system tick which allows the processor to continue sleeping when there are no application tasks to execute. Stopping the tick interrupt allows the microcontroller to remain in a deep power saving state until either an interrupt occurs, or the RTOS kernel has to transit a task into the ready state. This can make a huge difference in battery life. Tickless support can be added to any embOS project and is available with the latest version of Segger's embOS real time operating system. Segger provides application notes for tickless support for different CPUs.



LeCroy's 1-GHz, 10-Gsample/sec scope is under €10k

Teledyne LeCroy's € 9,990/£ 8,640 WaveSurfer 10 oscilloscope hosts the company's MAUI user interface, 10 Mpts memory, 10 Gsample/sec sample rate and advanced debug tool kit. Built on the WaveSurfer platform of large screen, small footprint oscilloscopes, the WaveSurfer 10 has a 10.4 in. touch screen display and compact form factor. The instrument has a wide variety of serial data protocol decoders, as well as a full complement of advanced active probes. LabNotebook documentation and report generation tool provides a fast way to save waveforms, save setups and screen images,

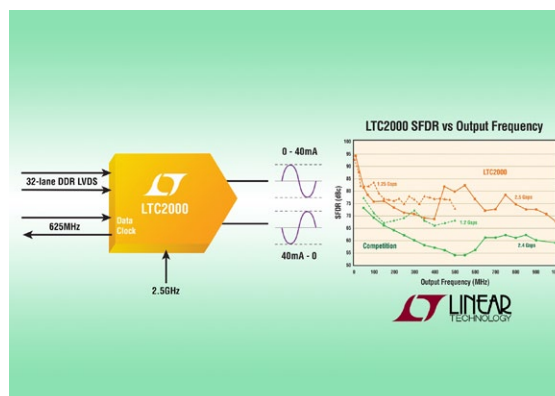


report results, and view offline. For debug and analysis, the sample rate of 10 Gsamples/sec on all four channels, 32 Mpts of memory, sequence mode segmented memory, history mode waveform playback, 13 additional math functions, and 2 simultaneous math traces - all included in the debug package, enable the WaveSurfer 10 to perform advanced analysis on long captures with 10x oversampling to find the root cause of problems.



16-bit, 2.5 Gbps DAC with 74dB spurious-free dynamic range

LTC2000 is a 16-bit 2.5 Gsample/sec DAC with very high spectral purity of 74 dBc SFDR at 200 MHz output, and better than 68 dBc SFDR for output frequencies from DC to 1 GHz, a 12 dB improvement over alternative 14-bit DACs. The LTC2000 has low phase noise and a wide 2.1 GHz, -3 dB-point output bandwidth, enabling broadband or high frequency RF synthesis in applications such as high-end instrumentation, broadband communications, test equipment, cable TV DOCSIS CMTS, and radar. Linear Technology comments that in such applications, the DAC is usually the bottleneck in meeting demanding specifications, and that the LTC2000 relieves those pressures by offering a new level of spurious [generation] performance, over 1GHz bandwidth, very



high linearity, and excellent accuracy. The ±1V compliant outputs feature a 40 mA full scale current which can be adjusted as low as 10 mA or as high as 60 mA to suit the application. Data is transferred to the LTC2000 over a parallel LVDS interface port with transfer rates of up to 1.25 Gsample/sec using a 625 MHz double data rate (DDR) data clock. Dual DDR ports are required to achieve the 2.5 Gsample/sec update rate, while a single port can be used to operate at a lower 1.25 Gsample/sec update rate. At 2.5Gsample/sec, the LTC2000 consumes 2.2W from dual 1.8V and 3.3V supplies, while at 1.25 Gsample/sec the device consumes 1.3W.



A rethought PIC IP core for FPGA or ASIC, with PIC compatibility

Polish IP Core vendor Digital Core Design has released its DRPIC1655X IP Core, which is compatible with the industry standard PIC16XXX, but claims four-times faster architecture and single-system-clock instruction execution time. DCD says that thanks to its price and software simplicity, engineers can minimise software development costs and enable easy portability across low to high-end platforms. DRPIC1655X is a low-cost, high performance, 8-bit, fully static soft IP Core, intended to operate with fast, dual ported memory. It has been designed with special attention to low power consumption, for an optimal power, price and performance combination. The company sees it as suiting IoT projects where, according to Jacek Hanke, DCD's CEO, efficient solutions like DRPIC1655X are the right answer, as they can be implemented for less than \$1 in 10k quantities. An FPGA netlist is also available. The

DRPIC1655X soft core is software-compatible with the industry standard PIC 16XXX (8-bit) MCUs. The architecture is four-times faster than the standard architecture; most instructions are executed within one system clock period.

The DRPIC165X is delivered with a fully automated testbench, complete set of tests and DoCD on-chip hardware debugger, which allow easy package validation, at each stage of an SoC design flow.

Unlike other on-chip debuggers, DoCD provides a non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, SFRs, including user defined peripherals, data and program memories.



Audio analysers give deeper insight into device performance

Analysers by Audio Precision are found in many R&D and production environments where high-performance audio systems are designed and built; now, a new generation which claims the lowest-available residual THD+N offers audio professionals unparalleled insight into their designs.

added different user operating modes to simplify making exacting audio measurements in both manually-driven, lab-environment; and in programmed, operating environments.

The APx555, AP says, has improved measurement accuracy, speed, flexibility, automation and ease-of-use for developers



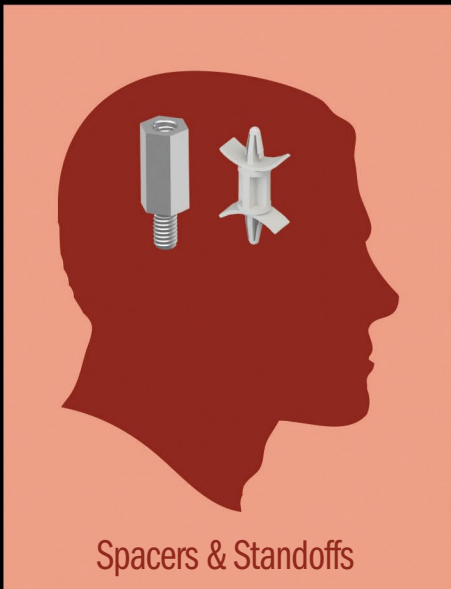
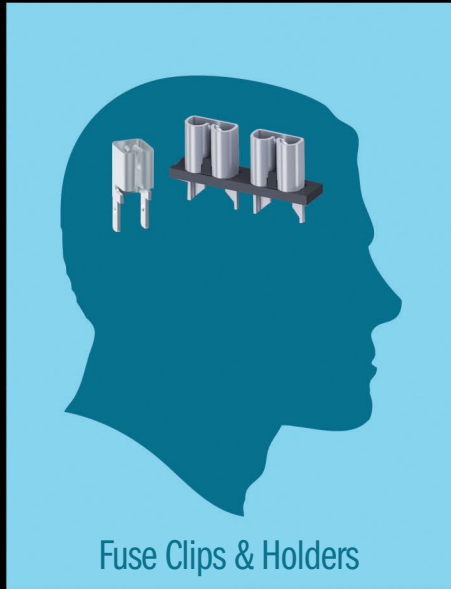
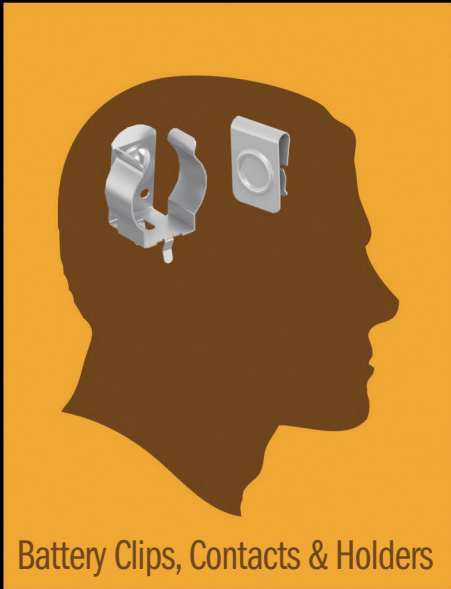
Audio Precision has two primary analyser product lines; the APx and the 2700 series. The former has been focussed on ease-of-use, on programmability, and has had what has been regarded as a simpler user interface. It (the APx) has tended to be used more often in a production environment, or for general 'trouble-shooting' duties. The 2700 series has been the company's highest-performance unit: as Audio Precision notes, one of the critical parameters of such an instrument is how much (or how little) distortion is introduced by the measurement process itself. The 2700 has been the company's 'flagship' for lowest total harmonic distortion plus noise (THD+N) figure. Now, with the APx555, the company has combined those attributes in one unit; it has increased THD+N performance and

of audio components, equipment and systems. With a typical residual THD+N of -120 dB (conservatively specified on its data sheet at -117 dB), the two analogue channels of the APx555 claim to add the lowest noise and distortion of any audio analyser yet built. This performance is coupled with 1 MHz bandwidth (mono) and an FFT resolution of 1.2 million points. AP notes that 24-bit resolution is maintained to 1 MHz. The generator is capable of producing low distortion sine wave signals up to 204 kHz, at high-level amplitudes up to 26 Vrms. This increases the user's confidence that the results they see owe nothing to the test system itself.



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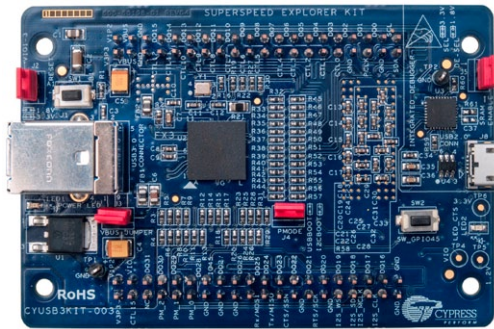
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Check out USB3.0 with low-cost dev kit

Cypress Semiconductor has a \$49 “SuperSpeed Explorer Kit” to accelerate USB 3.0 designs; the development platform enables designers to add high-performance USB 3.0 throughput to virtually any system. Cypress says. It is based on Cypress’s programmable EZ-USB FX3 USB 3.0 peripheral controller, which is positioned as the industry’s only programmable USB 3.0 peripheral controller. It is equipped with a configurable General Programmable Interface (GPIF II), which can be programmed in 8-, 16-, and 32-bit configurations. GPIF II allows FX3 to communicate directly with application processors, FPGAs, storage media, and image sensors and provides a data transfer rate of up to 400 MB/sec, while using lower power than alternative solutions. The SuperSpeed Explorer Kit easily interfaces with external devices via three accessory boards that connect to Aptina image sensors, Altera FPGAs and Xilinx FPGAs, respectively. The kit also includes an



integrated debugger with a standard USB interface to further simplify designs and speed time to market.

Cypress is also referring designers to the book “SuperSpeed Device Design by Example” by USB expert John Hyde at

IDF. “I have been working with many of Cypress’s FX3 customers and wrote my book to address their most common concern of ‘getting started,’” said Hyde, who’s also a principal at USB Design By Example. “The book covers the end-to-end development process including Windows examples, FX3 firmware examples, GPIF II examples, and even Verilog examples for a CPLD plug-on board that enables you to try a variety of high-performance interfaces to your own hardware.

I wanted to make SuperSpeed USB technology more accessible and believe that the book, along with the new Cypress kit, is a good first step in that direction.”

Complete article, here



The Wellness Measurement MCU, for health monitoring

Maxim Integrated has released the data sheet for an ARM-based microcontroller that uses an ultra-low-powered core, combined with the front-end processing appropriate to vital-signs measurements, specifically tailored for the wearable sensor/ “wellness” monitoring device market. The MAX32600 also incorporates advanced hardware security. It is based around an ARM Cortex-M3 32-bit RISC CPU operating at up to 24 MHz, with 256 kB of flash memory, 32 kB of SRAM, a 2 kB instruction cache, and integrated high-performance analogue peripherals. The profile of this implementation of the ARM core includes 175µA/MHz active power executing from cache, for low system power, and less than 1.0µA in low-power mode 0 (LP0).

The chip needs a digital supply voltage of 1.8V to 3.6V, and

an analogue supply of 2.3V to 3.6V. There is a range of digital peripherals, timers and interfaces, including SPI and I²C; the analogue front end (AFE) includes a 16-Bit ADC with Input Mux and PGA, that can run at up to 500 ksamples/sec; and a programmable-gain amplifier with gain of 1, 2, 4, and 8 and bypass mode.

A 6-Channel DMA engine enables intelligent peripheral operation while the MCU core is in sleep mode. Security features for data integrity and IP protection comprise a Trust Protection Unit for End-to-End Security; an AES Hardware Engine; MAA For ECDSA and RSA; Hardware pseudo-random number generator; and fast-erase SRAM for secure key storage.

Complete article, here



Design win; Nordic’s Bluetooth in a minimalist beacon design

“In contrast to many beacons on the market today that carry in our view a lot of unnecessary technological overhead, we partnered with Nordic to strip out as much complexity as possible out of our Pucks to maximise battery life and minimize cost and complexity,” explains CEO of Canadian startup, Reteneo, President, Jean-Christophe Titus. Reteneo’s stripped-down iOS and Android-compatible beacon platform supports \$15 per month subscription model and is based on – in fact, contains not much more than – a Nordic nRF51822 SoC. The Reteneo Pucks themselves are the size of regular [ice] hockey pucks and feature nothing more than a Nordic nRF51822 SoC, antenna, and two watch batteries. The ultra low power operat-

ing characteristics of the nRF51822 will allow the puck to run for an average of two years in continuous operation. Reteneo says another major benefit of the Nordic nRF51822 SoC is its ability to do firmware updates over-the-air, a platform feature that Reteneo plans to include in the future. The ‘Puck’ platform is designed to allow multiple retailers and merchants to offer beacon-based services to consumers via a single ‘Reteneo Life’ app instead of having to download a separate app for each beacon. Reteneo Pucks continuously advertise their presence to any passing iOS or Android Bluetooth Smart Ready smartphone within a range of up to 100m.

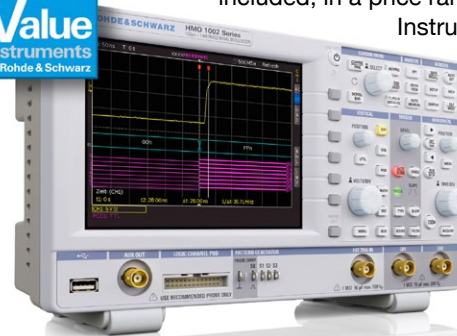
Complete article, here



Hameg/Rohde & Schwarz' entry-level, mixed-signal scope

Fanless operation, 1Mpoints of memory depth and a 1 Gsample/sec realtime sampling rate are the key features of the R&S HMO1002 mixed signal oscilloscope. With a vertical sensitivity of 1 mV/div and integrated 128 kpoint FFT, the instrument has a high specification for the “three-figure price segment”. Developed by Rohde & Schwarz subsidiary HAMEG Instruments, the units can be expanded at any time from 50 MHz to 70 MHz or 100 MHz bandwidth by means of a simple upgrade option. Measuring analogue and digital signals simultaneously may not be anything unusual for an oscilloscope these days, but it is, says the company, for a T&M instrument in the three-figure price segment (which we take to mean, below-€1000). Fanless design of the R&S HMO1002 is ensures quiet operation and makes the instrument less susceptible to faults. The oscilloscope's antiglare display takes up approximately 40% of the front-panel area and is easy to read. A logic probe can be connected to the front panel. An integrated pattern generator enables professional embedded developers to program protocol messages at up to 50 Mbit/sec. Full story [here](#).

Value
instruments
by Rohde & Schwarz



Also from the same maker comes a budget range of lab power supplies. Tracking, sequencing, and FuseLink are additional functionality included in the HMC804x series. Data logging and an integrated energy meter are further features that are included, in a price range below €1000. Also by Hameg

Instruments they are equipped with one (HMC8041), two (HMC8042) or three (HMC8043) channels. All models from this series deliver up to 100W and are adjustable between 0 and 32V in steps of 1 mV. Tracking is available in the two multichannel models and enables combined parallel or serial operation. It is still possible to provide power to several circuits independently. Changes to current and voltage values are carried out synchronously in combined channels. FuseLink is based on a

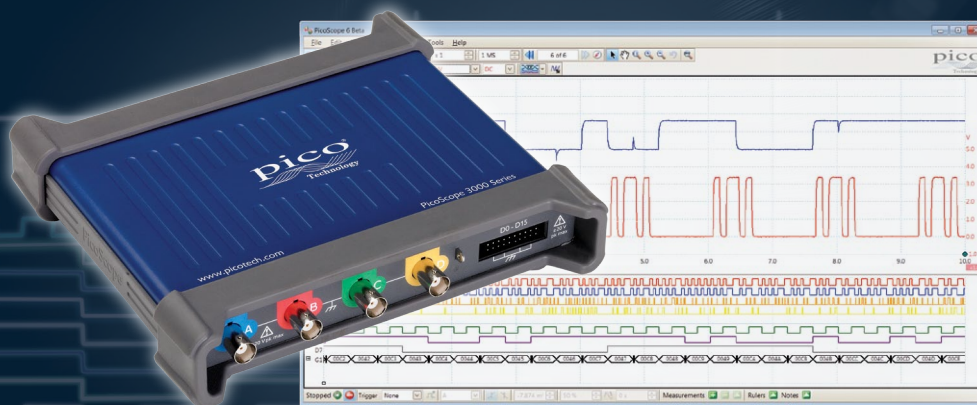
similar idea. This function combines the safety switch off current limits for multiple channels. If a channel exceeds its limit, the combined channels also shut off.



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IMPLEMENTATION OF A WIRELESS DATA TRANSMISSION PATH

In an intelligent factory equipped according to Industry 4.0, a central controller monitors and controls all areas, not only manufacturing.

Through wide-area use of smart sensors and actuators, manufacturing processes may be optimised and aspects such as security (access control, safety at work), energy efficiency (lighting and temperature control) and even connection to the smart grid may be controlled. Various wireless standards, optimised for certain applications, are available for the different tasks. To simplify data exchange between wireless networks and the central controller, Internet protocol based protocols find applications in the wireless world.

Progressive miniaturisation has produced very tiny sensors.

They may be deployed, among other scenarios, for monitoring and controlling machines with much enhanced accuracy. One example of this would be using Hall sensors (e.g. the TLE499x line of Infineon) for constant monitoring of all moving machine tool shafts. These may be used to monitor speed and play of the shaft. The power consumption may also be calculated based on the revolutions. Smart grid linking can help to reduce the power consumption by adapting speeds as necessary, even for individual process steps. By measuring shaft play, wear may be diagnosed earlier and equipment servicing scheduled to suit production.

Automatic temperature monitoring in the food industry is another potential application. An infrared thermometer may be fitted at the cutting table to document the integrity of the cooling chain.

Both examples demonstrate new possibilities for collecting information using small sensors, allowing more accurate control and monitoring. For data transmission between sensor network and controller, data must be translated to the relevant protocols when the transmission system changes. The gateway links the two systems. Since data must be transmitted bidirectionally, the translation turns out somewhat more complicated. Equipment available on the market is therefore generally expensive and not intuitive to use.

A gateway for data exchange between the server in the manufacturing facility and the sensor must therefore be able to integrate data into the relevant protocols bidirectionally. The wireless transmission standards are all based on the IEEE 802.15.4 protocol. Data transmission via the Internet is based on conventional Internet protocols. When the Internet was born, addresses were defined using 32 bits. Available addresses have in the meantime run out, however, since the number of Internet capable devices has increased enormously. To solve this prob-

lem, Internet protocol Version 6 (IPv6) uses a 128 bit address. This suffices to (proverbially) “allocate an IP address to each grain of sand”.

The gateway’s task of translating data between Internet and IEEE 802.15.4 protocols presupposes a powerful processor and a plethora of data processing routines. Addressing poses another challenge in a large network of sensors and actuators. The server sends data to the gateway’s IP address. The gateway extracts the address from the data stream and integrates the data into the relevant wireless protocol for transmission.

A gateway must work with several wireless standards, e.g. ZigBee for transmission of data from many intelligent sensors and WiFi for data intensive sensors such as cameras.

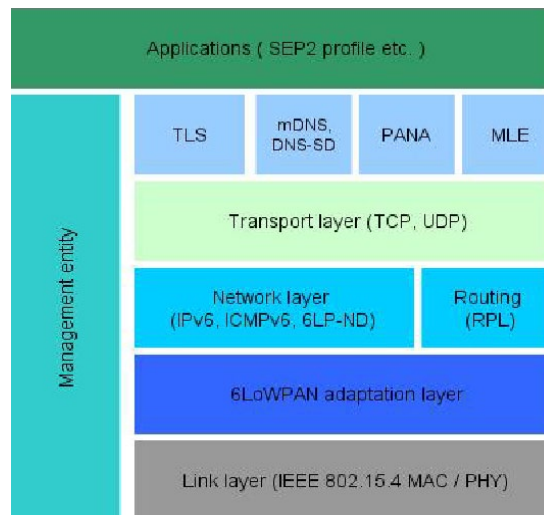


Figure 1. ZigBee IP protocol levels (Source: ZigBee IP Specification, Rev. 32)

To simplify data exchange between the various wireless protocols and the Internet, 6LoWPAN [IPv6 over low power wireless personal area network] has been developed. The protocol allows the 128 bit IPv6 address to be compressed via an IEEE 802.15.4 compliant protocol for data transmission. The data are furthermore integrated at the sensor already into one of the most common Internet transmission protocols, TCP or UDP. Like ZigBee, 6LoWPAN is capable of building a network of several paths between sensors.

The ZigBee Alliance has integrated 6LoWPAN into ZigBee IP. Figure 1 shows the protocol layers.

The IPv6 based wireless data transmission methodology is evident in the ZigBee IP structure. After the link layer, which transmits the data via radio waves, IPv6 compresses/decompresses the data using 6LoWPAN. The data transmission destination is determined in the network layer. The type of data transmission is specified in the transport layer – via TCP (reliable, but slow) or UDP (fast, but prone to data loss). All other layers offer additional functions such as AES data encryption.

Bluetooth, in Version 4.1 with the “logical link control and application” (L2CAP) function, also creates a basis for IPv6. This allows data transmission via separate channels.

But even with an IP-based standard like this, capable of devolving protocol administration for wireless and Internet-based data transmission to hardware, many issues remain to be addressed before a finished product can be launched into the market.

In the conclusion of this article, the author briefly considers some of the options available as connectivity modules – click right.





Analog Tips

ROUTING HIGH-SPEED JESD204B LANES

BY IAN BEAVERS

The JESD204B standard, which specifies a high-speed serial interface for data converters, supports a maximum speed of 12.5 Gbps. With ADCs and DACs offering several JESD204B lanes of data, the complexity of maintaining signal integrity can create a challenge for system engineers. In a JESD204B interface, the channel acts as a low-pass filter due to the capacitive effective of the PCB traces on the dielectric material of the board. Transmitter pre-emphasis, de-emphasis from the transmit output, and receiver equalisation can effectively boost the high-frequency content at the end receiver. The result is a nearly flat frequency response through the transmission with a lower risk of bit errors across the link.

Pre-Emphasis

A normal unaltered channel exhibits a frequency roll-off relative to the trace length and board materials, while a channel using pre-emphasis provides high-frequency boost and acts like a high-pass filter, compensating for the loss by boosting the signal over the nominal peak-to-peak voltage (Vpp) levels. Thus, the system response on the pre-emphasis channel is balanced due to amplification of the high-frequency content. A channel using pre-emphasis has a larger signal on certain bit transitions than does a channel without pre-emphasis, causing a high-frequency boost. This mitigates the effects of low-frequency roll-off, allowing data to be transmitted longer distances.

De-emphasis

De-emphasis normalises the signal so that Vpp remains the same for all bit widths, at the expense of a smaller Vpp at particular bit transitions, as determined by a data look-ahead method. A channel using de-emphasis has a smaller signal Vpp than the original at certain bit transitions. De-emphasis can compensate for inter-symbol interference that can occur on "runt pulses," which tend to show the first mask violations on an eye diagram.

Equalisation

JESD204B receiver equalisation provides high-frequency boost for the frequency roll-off of the channel. Pre-emphasis and de-emphasis methods require knowledge regarding future transitions of the incoming data that is not available at the PHY receiver. Instead, the equalisation block at the receiver is a high-pass filter that compensates for the low-pass frequency-dependent effects of the channel. JESD204B transmitters and receivers with both emphasis and equalisers can work together to extend the insertion loss in a mutual manner compared to using only emphasis on the transmitter, or only equalisation on the receiver.

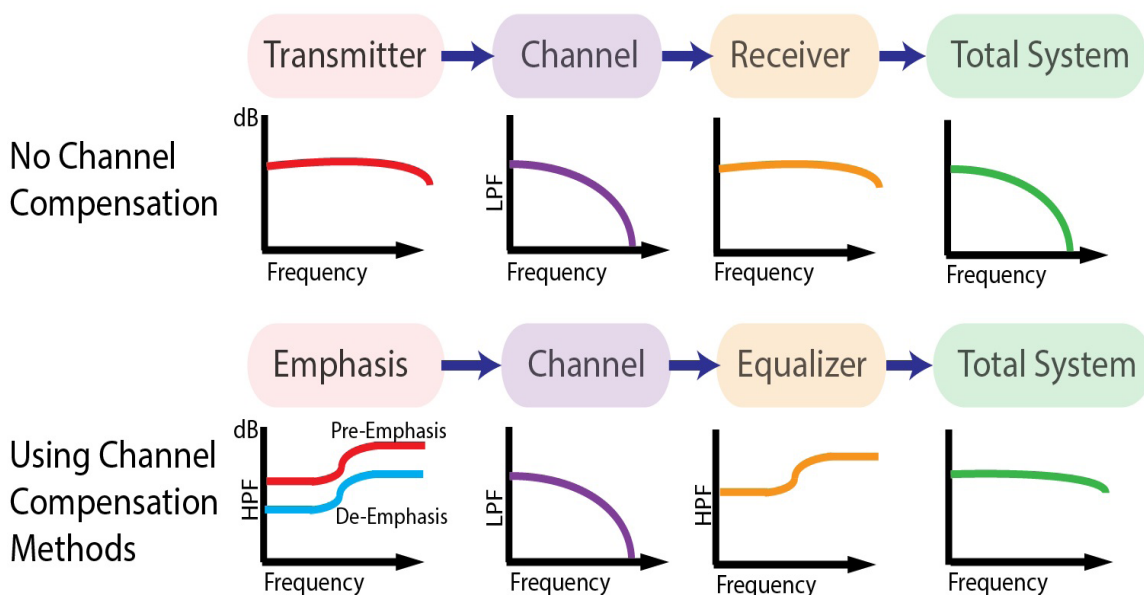


Figure 1. System frequency response compares uncompensated (top) and compensated channels (bottom).

About the Author

Ian Beavers [ian.beavers@analog.com], a staff engineer for the Digital Video Processing Group at Analog Devices (Greensboro, North Carolina), is a team leader for HDMI and other video interface products. With over 15 years' experience in the semiconductor industry, he has worked for ADI since 1999. He holds a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro.



SOFTWARE BOTTLENECKS NECESSITATE INNOVATIVE DEVELOPMENT TOOLS

As the complexity of modern embedded systems continues to rise at an almost exponential rate, the exacting demands placed onto engineering teams are piling up. More sophisticated memory systems with varying sizes and access latencies are now starting to be incorporated into designs. Multi-core processors are also becoming more commonplace. The question is - are developers adequately equipped to take on the challenges that lie ahead?

Producing a working software system within project timescales and budget constraints is of paramount importance. These aren't the only challenges of course. Engineers also need to maximise the efficiency of their design to gain a competitive advantage. They must undertake optimisation in relation to a variety of key parameters, such as:

- Completeness and feature set of their design
- Hardware cost
- Code size
- Performance level
- Power budget

The way in which optimisations are applied is still relatively crude in comparison to the cutting-edge embedded systems being designed. Existing code generation tools make optimisations using processor-focused instructions, but these are, as a result, inadequate for anything but the most rudimentary of sequences. The numerous interactions between the processor/memory have the greatest influence over the performance of an embedded system, so these should be appropriately addressed. Traditional tools try to identify the most common control flows through a program then optimise for this dynamic behaviour at the expense of other, seemingly less important control flows.

However in reality, programs exhibit highly dynamic behaviours, and even infrequently-taken control flows can make dramatic changes to the processor/memory state, which affect the behaviour of other flows. Profiler tools can provide developers with information on which system resources are being expended (such as memory bandwidth, cache hits/misses, etc.). However, this isn't the whole picture - it says nothing about the fundamental causes. The interactions of software and hardware are so complex in modern processor systems it is just too difficult for programmers to directly control many of these effects from their source code. Comprehending the underlying relationships at work here is frequently beyond the faculties of even the most skilled engineering professionals.

In reality there is a considerable gap between hardware's theoretical performance, and new hardware features such as high performance tightly-coupled memories, and what can be achieved with traditional software development tools. This is starting to cause major issues and, in many cases, unnecessary compromises are having to be made in order to alleviate acute time-to-market pressures. It is for such reasons the vast majority of design projects embarked upon do not manage to achieve their initial goals, coming up short of their true potential and not fully utilising the performance features available with modern hardware.

Optimising in the "bigger picture"

Programmers should concentrate on optimising the overall algorithm and architecture of their software. The fundamental problem at the heart of the software development tools' inadequacies is their inability to control low level hardware/software interactions and the requirement that there is still a "human in the loop" trying to optimise fundamental aspects of the software's execution by altering the source code.

Such efforts to remove execution bottlenecks using current optimisation techniques are poorly coordinated and lead to new problems being created elsewhere. This is akin to "balloon squeezing" - rather than making the balloon smaller it just pushes air around and causes bulges elsewhere. Even seasoned engineers will struggle to coordinate their efforts under such circumstances.

Scale and complexity of embedded software is increasing phenomenally

Development tools haven't evolved

It has become clear that the current approach taken is not capable of furnishing engineers with the level of functionality that they require. The tools available only encourage develop-

ment and optimisation procedures which are both unpredictable and time consuming. Engineers desperately need development tools which are more sophisticated, supporting hardware/software interactions and whole-program optimisations which can't be expressed in the source code, whilst also being much less labour intensive to use. This would give them the ability to reach more optimal designs while shortening the amount of time taken up by the project, the technical resources that need to be allocated to it and the associated costs. As well as curbing up-front investment, a major upshot of these shorter development cycles will be more rapid progression to the point when serious revenue can be generated by the end product.

There are now those who are starting to recognise that a deterministic, highly automated methodology to tackle hardware/software and whole system optimisations will allow the develop-

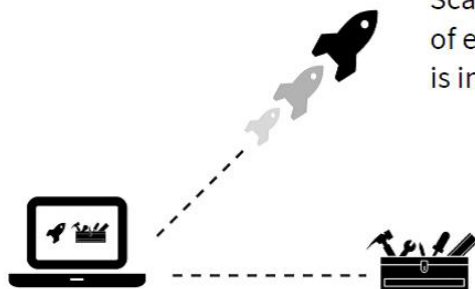


Figure 1. The problem, expressed in simple graphics terms - the increasing complexity of embedded systems vs. the relatively unchanging capabilities of current development tools.

ment process to be far more efficient. Engineers will have more time to exercise their creativity to the fullest, letting the tools automatically optimise their software into the available hardware resources.

Though existing whole-program compilation techniques are limited by their compatibility with widely deployed compilation/profiling systems and source code, advanced development tools are now starting to emerge that will offer the capacity to significantly enhance system performance and shorten the time needed to complete embedded design projects.

By ensuring the entire code generation flow is aware of the entire hardware, including the coupling of the processor and the memory system, optimisations embarked upon can achieve results that are beyond the scope of source code changes, existing tools and increasingly outdated manual techniques. Technology start-up Somnium is pioneering this approach. The company is working closely with leading semiconductor manufacturers to produce both generic and product-specific software development solutions that, in contrast to how current conventional optimiser solutions operate, carry out highly device-specific optimisations automatically without requiring any form of profiler feedback. The upshot of this is boosted productivity, with generation of programs which are smaller and more efficient for all dynamic behaviours.

In conclusion; embedded system designs often reach completion later than expected and are not successful in satisfying the various cost, performance and functionality targets that were set at the beginning. To a large extent, this is due to the widening disparity between what engineering teams are seeking to accomplish; and what their development tools can deliver.

The conventional manually-based procedure of design optimisation must be replaced by a process which can cope with the inherent complexity and in which the human element has thereby basically been eliminated. Instead of optimisation being centred totally on the processor element, the system as a whole must be examined, with the available on-chip and off-chip memory systems being key to the optimisation strategy.

The items discussed in this article all point to a compelling need within the industry for a new breed of software development tools which are 'device aware' and where both the code generation and data sequencing processes are automated in their entirety. Through efficient and deterministic optimisation, as proposed here, engineers can make much better use of the hardware they have at their disposal - so they can achieve more with less.

David Edwards is CEO/CTO and Founder, Somnium Technologies



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ISOLATING USB 2.0 AND POWER FOR HARSH ENVIRONMENTS

Connect your desktop PC to industrial or medical equipment using a standard USB (Universal Serial Bus) cable and you may quickly learn an expensive lesson.

Your PC and the piece of machinery can easily be connected to different outlets at different ground potentials. So after connection, the USB cable can provide a lower impedance ground path between both devices, enabling everything along the USB power path to fry. Replace the PC with a device that depends on USB power, such as a portable scanner, and your dilemma might be that you are faced with a USB port that provides insufficient power. Perhaps more frustrating is when you know all of your devices are safely connected and powered properly, yet the electrically noisy environment makes communications go haywire.

The USB standard was developed in the mid-1990s and was never designed to operate in a noisy environment. It was meant to connect low power peripherals to PCs over short distances in a relatively quiet home or office environment. Fast forward to today, where it has grown wildly popular for characteristics such as its speed and ease of implementation, designers rely on USB to interface computers with a wide variety of custom peripherals, where it has become clear that isolation is required in certain applications, especially in the medical and industrial arenas. Isolated USB transceivers are available in the market, but these solutions exclude isolated power and passive devices, forcing larger, more complex designs. A more elegant solution is an isolated USB transceiver and power, which drastically simplifies any isolated USB 2.0 hub or peripheral design and prepares them for harsh environments.

Chipscale isolation and power

Galvanic isolation is used in a variety of industries, most commonly to provide safety against potentially lethal voltages. Isolation is also used to eliminate the effects of noise and common-mode voltage differences created by ground loops, or as a level shifter between dissimilar operating voltages. Typically, building an isolated system requires a number of passive and active components on either side of the isolation barrier in addition to the barrier components themselves. Barrier components are notoriously difficult to use, adding significant design time and cost to isolated systems. With this in mind, Linear Technology developed a line of μ Module isolators that reduce the design of isolated systems to simply plugging in a module, with no complex barrier components required; these isolators require no external components at all. The LTM2884 USB μ Module isolator, shown in Figure 1, provides 2500 VRMS of galvanic isolation and integrates a USB 2.0 transceiver, a no-opto flyback converter, ultra-low quiescent

current LDOs and all required passives in a 15 x 15 x 5 mm surface mount BGA package.

The module employs inductively coupled coils, or coreless transformers, to pass data across the 2500 VRMS isolation barrier, while dedicated ICs perform the data transmission and receiving functions for both USB channels and both data directions. USB signals on either side of the barrier are encoded into pulses and translated across the barrier using differential signaling through the coreless transformers formed in the μ Module substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation.

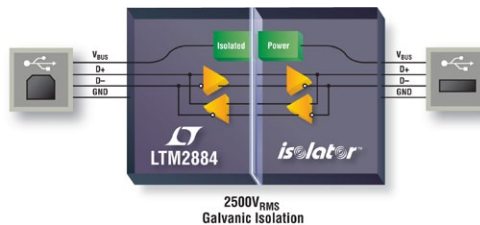


Figure 1. Isolated USB transceiver with isolated power

Isolated power in the module is generated by more conventional means. Power is derived from a boundary mode flyback converter with primary side voltage sense regulation. This overall power topology provides a simple, flexible, fault tolerant and relatively efficient design (~65%). The LTM2884 has two separate inputs for powering the onboard USB

transceiver and DC/DC converter. The USB transceiver accepts power from a 4.4V to 16.5V bus or external supply. The DC/DC converter also accepts power from the same sources; if connected to a 5V bus, isolated peripherals can harness up to 1W (200 mA at 5V) of isolated power; otherwise, connecting a greater-than-8.6V external supply provides peripherals with 2.5W (500 mA at 5V).

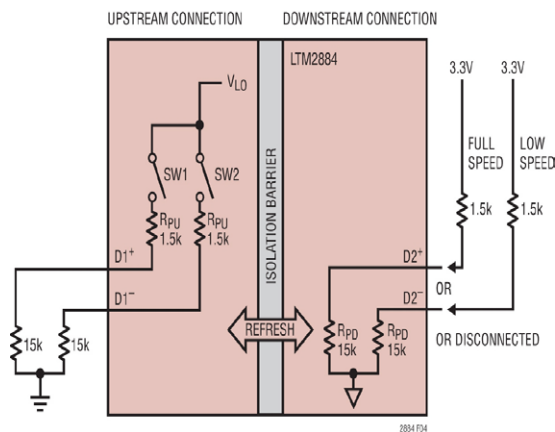


Figure 2. Automatic selection of internal upstream pull-up resistors to match downstream speed

Simplifying rugged designs

The USB path is compatible with both USB 2.0 full speed (12 Mbps) and low speed (1.5 Mbps) operation (figure 2). The device detects the speed of a connected USB device on the downstream port and then sets its own internal pull-up resistors on the upstream port to match the speed accordingly. Integrated pull-down resistors also support the downstream bus configuration. The LTM2884 maintains the conditions of the USB bus idle state by monitoring

the downstream idle condition and refreshing the state across the isolation barrier at a consistent rate. If the upstream port is idle for greater than 3 msec, the module can enter suspend mode to reduce its own power consumption to less than 500 μ A. This automatic speed selection feature eliminates the need to set jumpers or configure software, enabling truly plug-and-play designs.

Read on, regarding ESD protection and EMC performance, and some on-board deployments already in place – click right.





Eye on Standards

Four 400G quandaries to look forward to

By Ransom Stephens

The 400 GbE (that's Ethernet at 400 Gbits/sec to you and me) task force has convened and hopes to deliver a 400GbE specification in Q1 of 2017. At this time, everything is on the table. In [400G Ethernet Effort Begins](#), John D'Ambrosia, Chair of the Ethernet Alliance and 400G Ethernet Group, said, "The key part is that this initial effort will spend significant time and energy on defining an architecture that will be flexible and enable future 400GbE implementations." He went on to say that, "diving into the technical details of each of these anticipated proposals will be part of the fun that awaits those ready for this project."

Back in 2007, the [IEEE 802.3 High Speed Study Group](#) realised that the data rate needs of networking and computing have been increasing at different rates (Figure 1); Moore's Law scaling of 2x every 18 months for networking and 24 months for computing. So even though the 100 Gbit/sec spec is still somewhat incomplete, the technology is being rolled out and it's not hard to see the demand for 400 Gbit/sec links coming on the horizon.

Among its goals, the 400G working group hopes to maintain backward compatibility, preserve Ethernet frame formatting, support OTN (optical transport network), and specify EEE (energy efficient Ethernet) as an option.

In addition to increasing the media access (MAC) rate by a factor of four over 100 GbE, the IEEE 802.3bs 400 GbE group plans address the following four quandaries.

Improving the maximum permissible BER (bit error ratio) by a factor of ten, from 1E-12 to 1E-13.

Improving BER performance is likely to require implementation of FEC (forward error correction) embedded in the PCS (physical coding / reconciliation sublayer) so that the FEC isn't befuddled by more errors than it can correct in a span. The idea is that the PCS gearbox

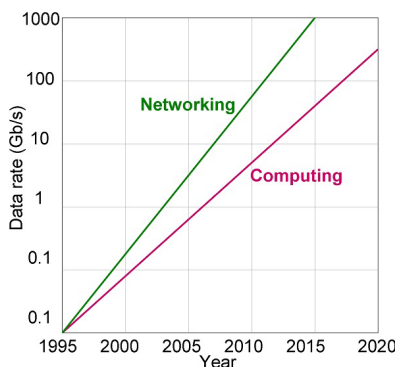


Figure 1. Core networking and server i/o demand projections from 2007 show that networking speeds are increasing at a faster rate than computing speeds. Source: IEEE 802.3 HSSG.

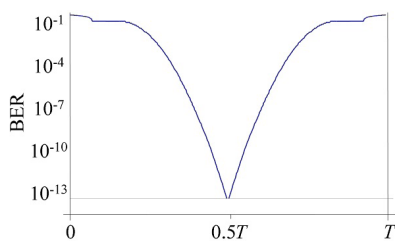


Figure 2. Bathtub plot for a signal operating at BER = 1E-13.

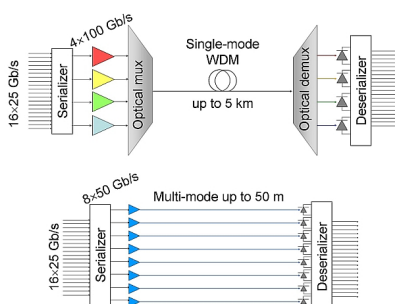


Figure 3. Two of many possible 400G topologies.

essentially stripes the data so that FEC isn't faced with too many errors per frame even in the presence of bursts. The expectation of burst errors comes from the tendency of current state-of-the-art receiver DFE (decision feedback equalisation) to burst when it fails. Figure 2 shows a bathtub curve for a system operating at BER=1E-13.

Expect the standard to specify minimum of 100m over multi-mode fibre and 5 km over single-mode fibre, with many different configurations.

The idea is to support a variety of topologies so that different technology options can be implemented to reach 400 Gbits/sec. A single 400 Gbit/sec optical signal on one fibre carrying one wavelength is unlikely. Rather, the back-to-the-future trend of parallel lanes that preserve the advantages of serial data systems will continue to proliferate from 100 GbE (Figure 3).

That is, we should expect combinations of WDM (wavelength division multiplexing, i.e., multiple independent wavelengths carried on a single fibre) and multiple fibre configurations. Since WDM performance is limited on multimode fibres, expect WDM single-mode fibre and parallel multi-mode fibre scenarios in almost every permutation of 25 Gbit/sec, 50 Gbit/sec, and 100 Gbit/sec links that can combine to 400 Gbit/sec. The permutations may range from the full-blown, long-reach, four wavelengths at 100 Gbits/sec on one single-mode fibre, to a stop-gap, early design of 16 separate multimode fibres each carrying a 25 Gbit/sec signal: and everything in between.

The continuation of this article looks at electrical chip-to-chip and chip-to-module channel options, and at possible modulation formats for the enhanced data rates.



A LEAP INTO QUANTUM COMPUTING

This is the first in an occasional series that will describe some of the current work being done, and challenges in the field of quantum computing. I will also use this soap box to attempt to intrigue fellow electrical engineers into considering the field as a viable area of research, as many of the challenges currently plaguing the field fall under engineering disciplines.

Now before I get too far into technical challenges around quantum computing, it seems prudent to give a quick run-through of the basics. Since there are already countless books, papers, and videos that offer a much better introduction and explanation of quantum computing than I would be able to, I will make it brief. I will focus on the Quantum Circuit Model, as it is much more relatable to classical computing, and can easily simulate most other quantum computing models.

Quantum Information Theory

The smallest unit of a quantum computer is the qubit, the quantum equivalent of the classical bit. As with the classical bit, a qubit can be in states 0 or 1, or more accurately represented as $|0\rangle$ or $|1\rangle$, using bra-ket notation (these are the basis states or basis vectors of the qubit, as can be seen below). One of the properties that makes the qubit unique, and more powerful than a classical bit, is that it can also be in a superposition of the two states, $\alpha|0\rangle + \beta|1\rangle$, where $|\alpha|^2$, $|\beta|^2$ represent the probabilities of each state being measured.

$$\begin{aligned} |0\rangle &= \begin{bmatrix} 1 \\ 0 \end{bmatrix} & |1\rangle &= \begin{bmatrix} 0 \\ 1 \end{bmatrix} & \alpha|0\rangle + \beta|1\rangle &= \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \\ |01\rangle &= \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} & |11\rangle &= \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} & \alpha|01\rangle + \beta|10\rangle &= \begin{bmatrix} 0 \\ \alpha \\ \beta \\ 0 \end{bmatrix} \end{aligned}$$

You can also consider the states of the qubit through the use of the Bloch Sphere (or the Poincaré Sphere for those in optics) as seen in Figure 1.

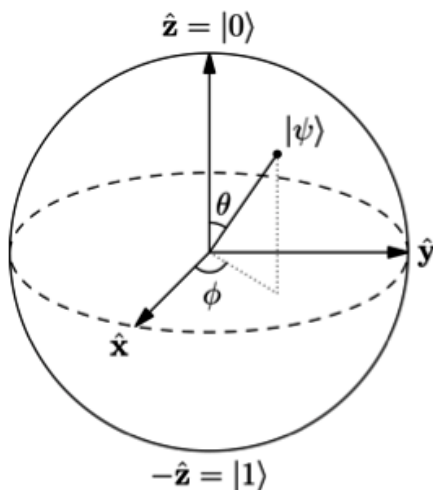


Figure 1. The Bloch Sphere [Ref. 1]

This is basically a sphere of radius = 1 in the three dimensional Cartesian plane, but with the y-axis being imaginary. Any pure state can now be represented as a point on this sphere (I specify pure state, as qubits can also be in mixed states, which is different from a superposition, but that is a topic for another time). If we are measuring in the Z basis, we can have $|0\rangle$ be +1 on the z-axis, and $|1\rangle$ be -1 on the z-axis, with the x- and y-axis representing superposition and phase.

The amount of time a qubit will remain in a given state before succumbing to noise and loss from the environment is called the decoherence time (as an example, how long a qubit will stay in $|1\rangle$ before it flips to $|0\rangle$). Different physical implementations have different decoherence times, but the very nature of the qubit results in there always being some decoherence.

This all might be starting to sound a little odd by now, but the important thing to remember is the qubit can be in a superposition of $|0\rangle$ and $|1\rangle$ and it will stay in a given state for a limited amount of time.

We can control a qubit by applying single qubit gates. These are equivalent to rotating our point on the Bloch sphere around one of the axes. One of the simplest is a Pauli-X gate (the quantum equivalent of a NOT gate), which rotates the point around the x-axis by π radians. If you are in the $|0\rangle$ state, the gate would change the qubit to the $|1\rangle$ state. This is not enough to do any useful computations, so gates that allow interactions between qubits are also required – such as the C-NOT gate – which operates in the same manner as the classical equivalent. One can see numerically how this works through representing the gates as matrices, as shown below.

$$X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad C-NOT = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

$$X \cdot |0\rangle = |1\rangle \quad C-NOT \cdot |11\rangle = |01\rangle \quad C-NOT \cdot \begin{bmatrix} \alpha \\ \beta \\ \gamma \\ \delta \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \delta \\ \gamma \end{bmatrix}$$

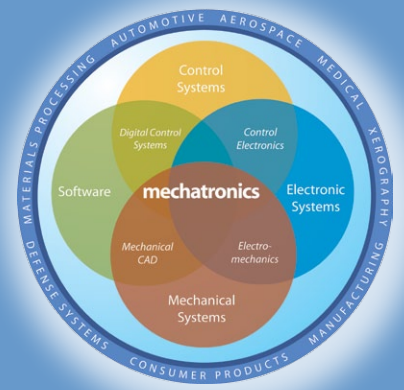
How such a gate is physically accomplished is dependent on which physical implementation of a quantum computer is being used, as analysis of the system's Hamiltonian (think of the Hamiltonian as an equation representing the total energy of the system) is required. However, we are in luck, as many of the engineering issues in the field can be understood without ever looking at a Hamiltonian.

Before concluding this initial foray in the realm of quantum computing, the author looks at how gates may be physically implemented – click right.



MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING
MECHANICAL SYSTEMS,
ELECTRONICS, CONTROL SYSTEMS,
AND SOFTWARE IN DESIGN



Gears in motion-control systems

Kevin Craig

Gears provide two main functions in motion-control systems. In power systems, they match the relatively low-speed, high-torque requirement of the load to the high-speed, low-torque, high-efficiency operation of the motor. Precision systems focus on transmitting motion as accurately and as repeatably as possible, as needed in robotic systems.

When the lessons of achieving higher precision are applied to power systems, greater efficiency, lower noise, and longer life can be achieved. As stronger and more wear-resistant materials and better lubricants are continually being developed, there is an ever-present need for new gears to be designed to pack more power into less space.

In addition, MEMS researchers are creating gears to solve the same problems that they face in the macro world. World renowned MIT design educator Alex Slocum relates an interesting anecdote: When a student design team was asked how their human-powered system was going to generate the required 600W power, when a human can only comfortably continuously generate about 100W, they replied “we will use gears.” The laws of thermodynamics still apply, even to gears!

The most frequently used gearings in high performance, closed-loop servo systems are spur gearing and planetary gearing. In spur gearing, the smaller gear is usually mounted on the input shaft and the larger gear is connected to the output shaft. A single pass is usually applicable to no more than a 15 to 1 ratio. Larger ratios are accomplished by using more passes. One

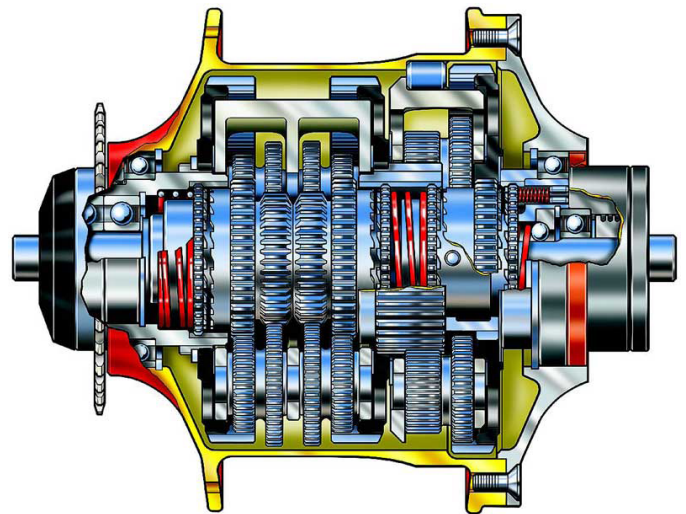


Figure 2. Cross-sectional view of the Rohloff Speedhub bicycle gearbox.

deficiency of the basic spur gear design is that in its simplest configuration, the input and output shafts are not in line, but a multi-pass unit design overcomes this.

Precision spur gearing are available with 98% efficiency up to a 100:1 ratio. Planetary gearing is a unique arrangement in which a set of four gears concentrically arranged around an in-line input/output shaft alignment is capable of providing much higher torque capacity in the same volume as a spur gear assembly. The three planet gears are driven by the sun gear (input) and are captured by the ring gear, which is machined into the gearhead housing. The three planets are in turn mounted on a spider assembly whose centre becomes the output shaft. Planetary gears can be fabricated in a multi-pass arrangement, as shown in Figure 1.

In approximately the same volume, the planetary gearing, compared to the spur gearing, can provide five to six times the torque, has a bearing structure that can support an average of 30 times the axial load and 15 times the radial load, and has an average of one fifth the backlash (the angle through which the shaft is rotated under the condition of no transmitted torque).

One doesn't have to look at complex machinery to find innovative gearing design. The Rohloff Bicycle Speedhub shown in Figure 2 is a planetary gear system. It has a gear range of 526% and the 14 gears shift in even increments of 13.6%. Machine design will never cease to provide opportunities for innovative-thinking engineers.

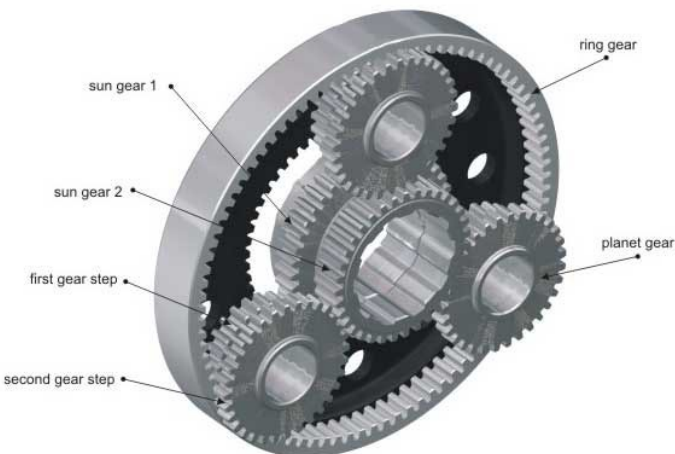


Figure 1. Outline of a planetary gear system.

THE G WORD: HOW TO GET YOUR AUDIO OFF THE GROUND (PART 3)

[Part 1 introduces the topic of grounding and "GND-think." Part 2 considers the ideal differential input.]

This article originally appeared in [Linear Audio](#), a book-format audio magazine published half-yearly by Jan Didden.

Impedance Balance vs. Current Balance

A confounding aspect of diff amps is that the input currents are almost never equal. Here's the situation. If I hold one input of a 10x diff amp at ground potential and drive the other, I get a factor 11 discrepancy in the input current, depending on which is the one that gets driven (Figure 15). And so, the unsuspecting engineer might naïvely reason, the input impedance is out of balance and should be put right.

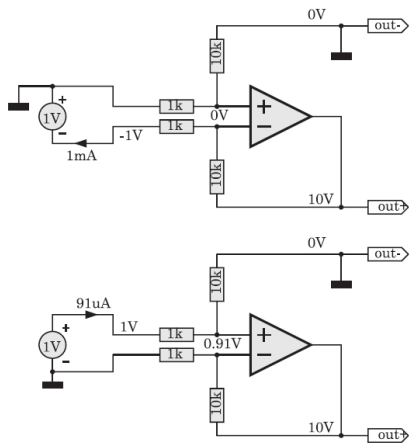


Figure 15. *The Imbalance Illusion.*

What they do in response to this misconception is quite ghastly (figure 16).

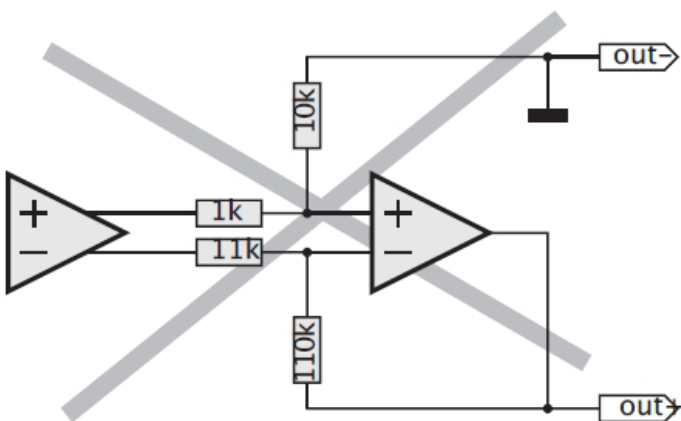


Figure 16. *Grisly outcome of cognitive illusion.*

You can easily see why there is something suspect about this. If, instead of driving the circuit with one leg grounded, we drove it with a symmetrical signal, the ratio between the input currents would no longer work out as 11:1 but as 21:1. You can't scale the impedances in a way that the currents work out equal under all conditions.

What's going on here? Remember to think of a differential input as forming a Wheatstone bridge along with the source

resistances. If you add source resistors to the above circuit you get something that is clearly no longer a difference amplifier as shown in figure 17.

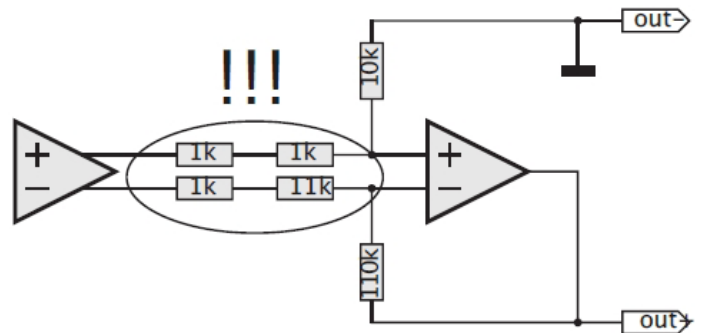


Figure 17. *Why it's grisly.*

We should repair the circuit and make the two legs equal again. We once again have a fully functional diff amp in figure 18. If the input currents are different, this is no indication of imbalance.

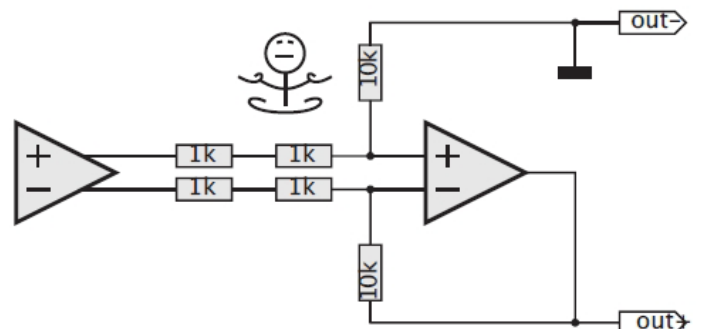


Figure 18. *Wei Wu Wei, or how balance is restored by not intervening.*

We should have seen from the start that the problem was illusory. In order to contrive it we had to drag the output reference of the difference amp into the equation and falsely assume that this is the point that the common-mode input impedance refers to. The circuit is balanced, certainly, but it just so happens that the input impedance references the virtual short, not some handy point that someone calls *GND.

Take-home messages

- Converting a circuit to differential does not require additional amplification stages.
- Each signal has its own reference.
- Making a circuit differential is not the same as building two independent copies of a ground-referenced one.
- Do not try to equalise signal currents. It doesn't work and you'll end up creating an impedance imbalance of heroic proportions.

Bruno continues by considering how the differential signal environment can be connected 'outside the box': [click right](#)



designideas

READERS SOLVE DESIGN PROBLEMS

Simple pulse oximetry for wearable monitor

Martin Jagelka , Martin Daricek & Martin Donoval

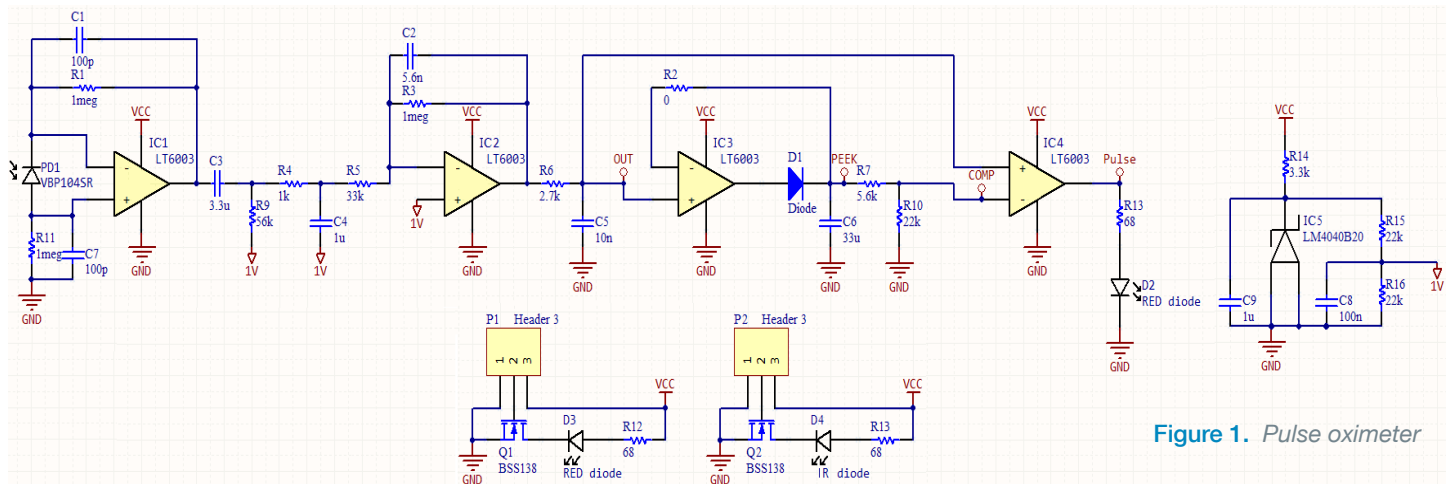


Figure 1. Pulse oximeter

Continuous monitoring of heart activity permits measurement of heart rate variability (HRV), a basic parameter of heart health and other diseases. This Design Idea is a new design of pulse oximetry that excels in its simplicity and functionality. Due to its capabilities, it can be used as a standalone device, able to



Figure 2. The time-dependent voltage output at nodes COMP (CH1) and Pulse (CH2)

monitor heart rate and oxygen saturation.

The core of the system is composed of the ultra-bright red LED (KA-3528SURC), infrared LED (VSMB3940X01-GS08), and a photodiode (VBP1045R) sensitive to both wavelengths of light at the same level.



Figure 3. The signal at node OUT

The basic building block of the system is operational amplifier LT6003, which is used in several stages. IC1 is used as a transimpedance amplifier, converting the current generated by the photodiode to a voltage. This stage provides high gain

and allows the use of the sensor on almost every part of the body. Op-amp IC2 is connected as an inverting amplifier with a gain of 30.

The negative input of comparator IC4 is connected to the modified signal using the peak detector circuit. Components IC3, D1, and C6 are used to detect and hold the maximum voltage of the input signal. R7 and R10 are discharging capacitor C6. This circuit is used for the reference voltage, allowing detection of even weak pulses caused by the sudden changes in position of the sensor on the body.

One high pass filter (HP) and two low pass filters (LP) are designed to filter out unwanted artefacts caused by external light changes or AC flicker. The HP filter and the first LP are set to a frequencies equal to 0.86 Hz and 159 Hz, respectively. Other terminals of both HP and LP filters are not connected to GND but to 1V reference, to increase the offset of the measured signal for further processing. The reference voltage is created by using the LM4040 and by the voltage divider (R15, R16). After IC2, the signal is processed in the second LP filter set at 5.9 Hz, which filters out other unwanted interference.

This short article does not explain the pulse reading process, which can be done by any MCU with an ADC. The MCU is needed for controlling the LEDs, signal measurement, and signal conversion into the oxygen saturation. Calculation of oxygen saturation is possible even with the narrow bandpass filter used. After turning the red LED on, the signal is measured by the ADC. After two or three pulses, the infrared LED lights up for the same period as the red one. The MCU uses the equation $S = V_R/V_{IR}$, where the voltages are the peak-to-peak readings, and S represents the value of StO_2 in a calibration table.

This work was supported by the Slovak Research and Development Agency under the contract no. APVV-0865-11 and contract no. APVV-0819-12 and VEGA 1/1177/12.

Optocoupler speed-up also reduces power consumption

Marian Stofka



Standard optocoupler speed is limited mainly by the relatively slow response of the phototransistor. This Design Idea adds components to the LED drive side to speed things up.

R1 is the original LED resistor, as used before the extra circuitry was added. Here however, its value can be higher, as the turn-on speed is determined mainly by the added circuit. You can thus save power, and also drive the LED with a less powerful driver.

The turn-on speed-up device is an emitter follower, NPN transistor Q1. The emitter follower has its emitter resistor split into a low-value part R_{EL}, and a higher-value part R_{EH} which is paralleled with capacitor C. At a steep rise of input voltage V_{IN}, the initially uncharged capacitor C temporarily “shorts” R_{EH}. Thus, the emitter current flowing through the LED has an increased value of:

$$I_E \approx \frac{V_{IN} - (V_{BE0} + V_F)}{R_{EL}}$$

Current I_E should not exceed 50 mA. For a step V_{IN}, the capacitor C charges roughly exponentially with a time constant of $\tau = R_{EL}C$. The value of capacitor C had been initially determined using:

$$C \approx \frac{t_{r0}}{2.3 \times R_{EL}}$$

where t_{r0} is the risetime at output of the bare optocoupler.

The obtained value of 13 nF results in excessive overshoot of output V_{OUT} however. The proper value of C was therefore determined experimentally to optimally be 1.5 nF, which results in a negligible 2% overshoot of V_{OUT}. Schottky diodes D1 & D2 serve for fast discharging of the capacitor C for an input falling-edge, and simultaneously for suppressing reverse bias at the base-emitter junction of Q1 and the LED.

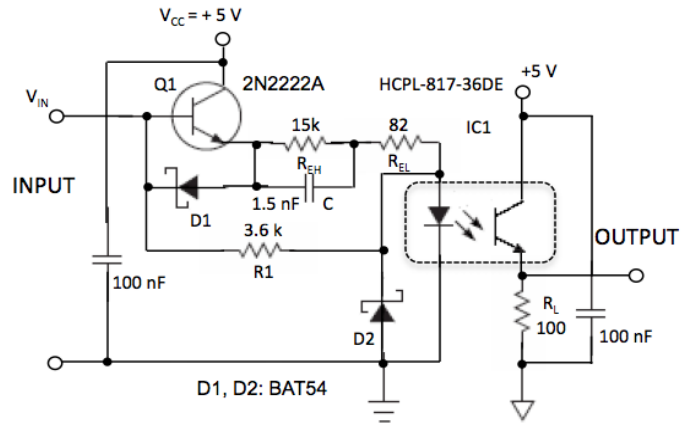


Figure 1. The speed-up circuit not only increases speed of propagation of a rising input signal, but achieves this speed-up at lower power consumption, compared to simplistic driving of the LED through a resistor.

The circuit has been tested at V_{CC} = +5V, and input step from 0V to +3V. The results obtained were: Turn-on delay t_{dr} = 0.5 μsec; full turn-on time t_{on} = t_{dr} + t_r = 2.8 μsec. For the optoisolator without the speed-up circuitry (R1 = 3.6kΩ), the values measured were 3.2 μsec and 10.8 μsec.

The conclusion is that the rising-edge delay has dropped due to the speed-up circuit to less than 1/6 of the unmodified coupler, and the turn-on time has dropped to roughly 1/4 of the original value. Note that these results were achieved while simultaneously lowering the forward current of the LED to about 0.5 mA, in comparison to the 5 mA listed in the datasheet of IC1.

Dr. Marian Stofka is with the Slovak University of Technology, Faculty of Electrical Engineering and Information Technology in Bratislava, Slovak Republic.

Short circuit tracer/finder uses low power

Dan Meeks



This Design Idea presents a low power short circuit finder that capitalises on the ear’s sensitivity to changes in frequency. The heart of the circuit is a voltage-to-frequency converter (based on Linear Tech’s AN45, Figure 13, by Jim Williams), which converts millivolt-level DC voltages to a wide range audio frequency output.

The excitation signal is created by low power DC-DC regulator U1. This circuit provides a 100 mV output, current limited to 100 mA by the 1Ω output resistor. This voltage should be low enough

that it won’t hurt or bias sensitive circuits.

Four-wire probes with Kelvin connections near the tips are used because of the low voltages. The bias current flows through the probes and the shorted part of the circuit, creating a very low voltage drop between the probe tips.

The Kelvin-connected sense wires apply that low voltage to the voltage-to-frequency converter (see LT AN45 for a description of that circuit). The frequency increases as the circuit resistance increases, and can be tuned to your preference using potenti-

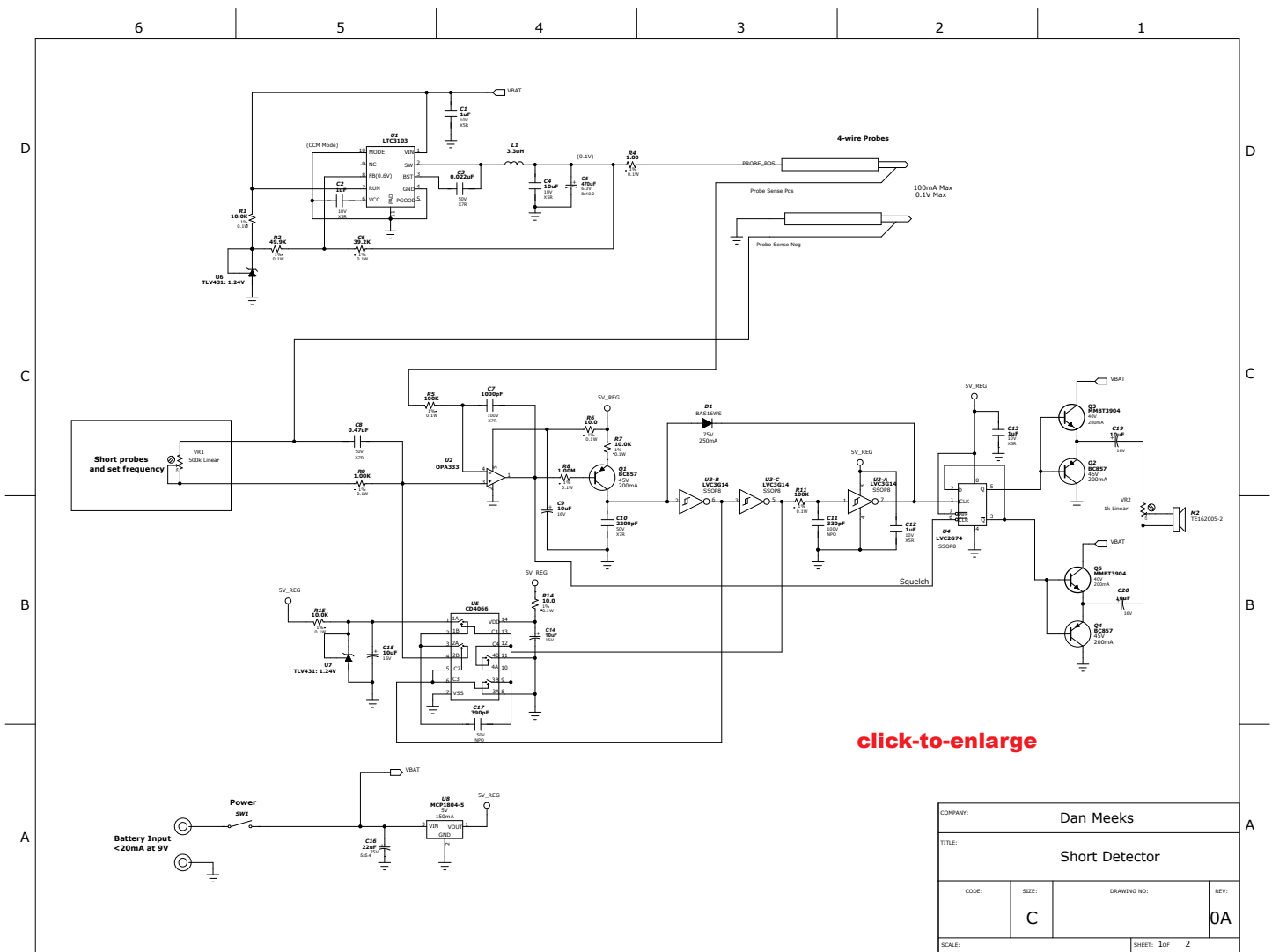


Figure 1. The short detector is based on a voltage-to-frequency converter; click to expand this diagram for full readability. NB; the resistor labelled 'C6' should read 'R3'.

ometer VR1. The output of the voltage-to-frequency converter is applied to flip-flop U4 to produce nice squarewave output signals to drive audio transducer SP1.

When the probes are removed from the circuit, the output frequency goes up to about 6 kHz. To prevent insanity, the output of the error amplifier, U2, is used to disable the audio.

To use the device, you first null the probes by probing the circuit that's shorted, and adjusting VR1 to a frequency that you like. Then, moving the probes along the conductor, the frequency will increase as you move away from the short, or decrease as you get closer to it. The pot provides a lot of frequency range so that it can be adjusted as desired. With the probes shorted together, the frequency can be nulled to zero. In that case, the sensitivity is about 100 Hz per milliohm. If the 0Ω frequency is adjusted to 1 kHz, the sensitivity is about 1 kHz per milliohm.

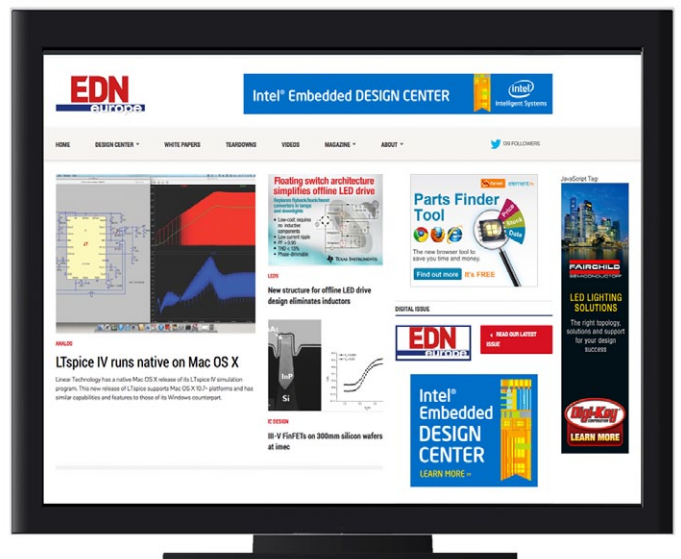
Operating current from a 9V battery is less than 10 mA when the audio is disabled (probes open), but with a reasonable audio level, the current is still less than 20 mA.

Dan Meeks is a Design Services FAE at Ion Associates, with a background in RF / Microwave, analogue, power, and embedded

control designs. After being a "real" design engineer, he worked as an FAE for Linear Technology and Texas Instruments.

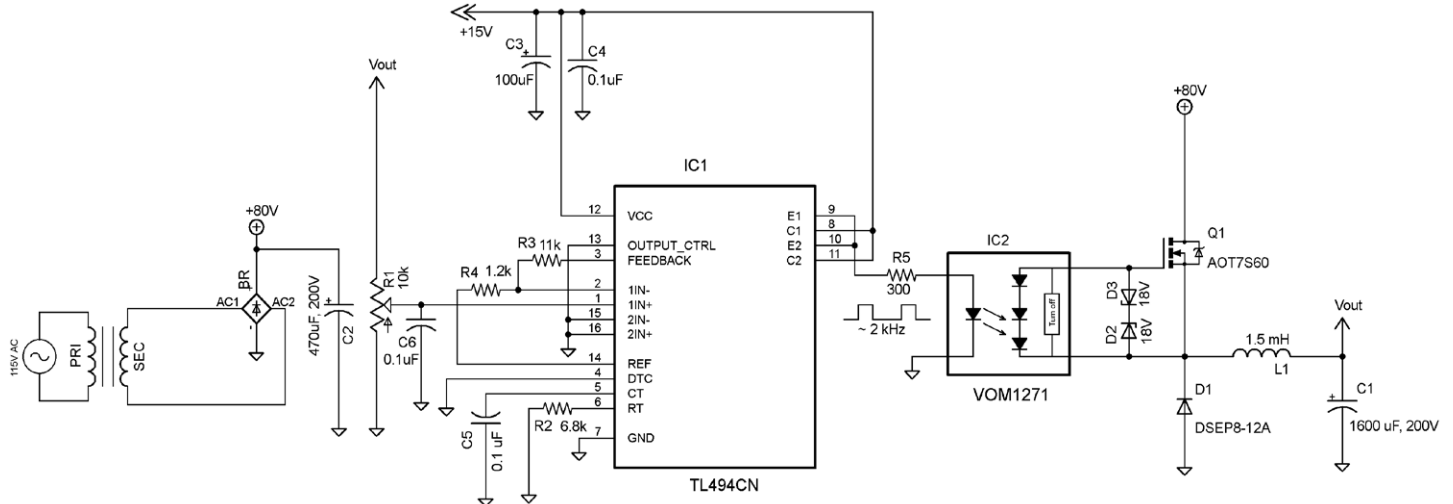
Also see:


[Milliohm Squawker](#) great at finding shorts and reverse engineering PCBs



Variable HV power supply employs photovoltaic optocoupler

Sajjad Haidar



 Power supplies with adjustable DC output ranging from 0V to 30V or 60V are on the market. Above 60V, there are not many. This Design Idea offers a solution.

There are many fixed voltage switching mode power supplies (SMPS) available, and connecting several in series can give us a higher fixed voltage. To obtain an adjustable output either from a SMPS or conventional transformer based supply, one needs to use a linear regulator or a switched mode buck converter. For a buck converter, a MOSFET or an IGBT can be used as a switching element.

Usually, for a high side switch, an IC with bootstrap operation or a pulse transformer is used. There are few photovoltaic couplers available to drive MOSFETs. As they do not provide much

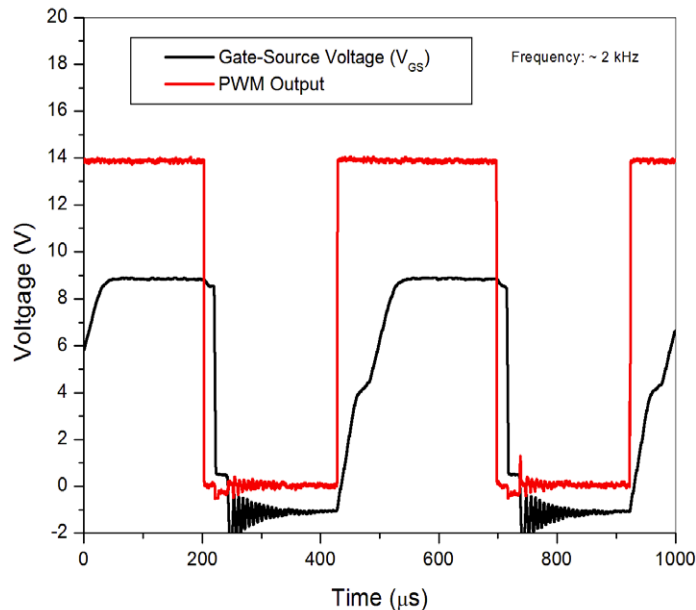


Figure 1 shows the gate-source voltage waveform and the IC1 output waveform at 70V output and 230Ω load.

Figure 1. HV buck converter schematic

current to charge the gate capacitance quickly, these photovoltaic couplers are mainly used to drive low frequency MOSFET switches, such as solid state relays.

Here, an attempt has been made to use a photovoltaic coupler (VOM1271) in a switching regulator. This coupler has a built-in fast turn-off device. With a gate capacitance of 200 pF connected to IC2, switching times t_{on} and t_{off} are 53 µsec and 24 µsec, respectively. Considering this, a switching frequency of 2 kHz was chosen for the buck converter. A Texas Instruments TL494 (IC1) was chosen as a pulse-width-modulation controller.

An AOT7S60 MOSFET was chosen as a switching element, considering gate threshold voltage ($V_{GS(th)}$), total gate charge (Q_g), drain-source voltage (V_{DS}), and drain current (I_D). As the VOM1271 can provide about 8.4V, $V_{GS(th)}$ should be well below this value; Q1's $V_{GS(th)}$ is 3.9V, and at 8.4V it is well into conduction. IC2 cannot deliver much current (typically 45 µA). To ensure switching speed and reduce switching loss, gate charge should be low. The MOSFET has Q_g of 8.2 nC.

The buck converter was tested with a step down line transformer output after being rectified and filtered as shown in Figure 1. The output voltage is continuously adjustable from 5V to 70V by varying R1.

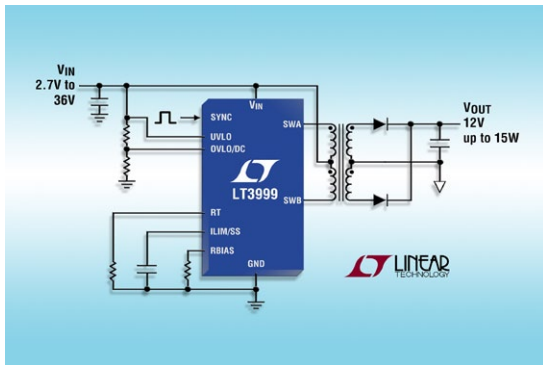
It is seen that though t_{off} is fast enough, t_{on} is about 80 µsec. This is considered to be a slow turn-on for many switching applications. However, for a switching frequency of 2 kHz, it should not cause much switching loss, especially for a load condition when the PWM duty cycle is large.

Though L1 has a smaller value than calculated for the range of output voltage, the ripple was 80 – 120 mVp-p for loads ranging from 80Ω - 230Ω. Ripple was 80 mVp-p at 70V output and 230Ω load. Line regulation was 0.75% at the same operating condition. Though the efficiency varies with the operating condition, the measured efficiency at $V_{OUT} = 70V$ and $I_{OUT} = 0.3A$ is 92%. Efficiency drops as output current decreases.

productroundup

36V monolithic 1A push-pull DC/DC transformer driver

LT3999 is a monolithic push-pull isolated DC/DC transformer driver with two 1A current-limited power switches, which operates over an input voltage range of 2.7V to 36V, is targeted



for power levels up to 15W and can produce a wide range of output voltages for automotive, industrial, medical and military applications. The programmable duty cycle

and turns ratio of the transformer sets the output voltage. The switching frequency is adjustable from 50 kHz to 1 MHz and can be synchronised to an external clock. The LT3999 input operating voltage range is set with precise undervoltage and overvoltage lockouts. The supply current is reduced to less than 1 μ A during shutdown. A user-defined RC time constant provides an adjustable soft-start capability by limiting the inrush current at start-up and an onboard cross-conduction prevention circuit increases reliability.

[Complete article, here](#)

Development kit to add NFC to MCU systems

The AS3911 NFC development kit includes an NCI standard-based interface to Android, Linux and Windows operating systems, providing a blueprint for an NFC implementation in



any microcontroller-based system. NFC can provide a simple, secure, wireless NFC interface between a microcontroller and the outside world. The AS3911

NFC development kit from ams eliminates the need for the OEM designer to implement a complete, proprietary software interface between a host microcontroller, its operating system and the NFC reader IC. The software in the AS3911 development kit includes an NFC Controller Interface (NCI) stack, a standard-based modular firmware/software solution, operating from the hardware level up to the operating system. Developed in collaboration with Stollmann E+V GmbH, it manages the interaction between a microcontroller and any NFC/HF reader in the AS391x family.

[Complete article, here](#)

8-bit PICs gain analogue blocks for capacitive touch

The PIC16LF1554/9 combines low power and dual ADCs with a hardware capacitive voltage divider (CVD) for capacitive-touch sensing, to reduce software overhead for advanced touch-sensing and general-purpose sensor applications. Microchip's 8-bit microcontroller (MCU) family has been augmented with the PIC16LF1554 and PIC16LF1559 (PIC16LF1554/9) devices. The PIC16LF1554/9 includes two independent 10-bit

Dual ADC With High-Channel Density and Hardware CVD



100 ksamples per second ADCs with hardware capacitive voltage divider (CVD) support for capacitive-touch sensing. This ADC configuration enables more efficient sensor acquisition and

assists with advanced touch-sensing techniques for extremely noisy environments, low-power applications, matrix keypads and water-resistant designs. The 14- and 20-pin PIC16LF1554/9 MCUs combine up to 17 ADC channels with automated hardware CVD modules.

[Complete article, here](#)

High-throughput USB-to-serial bridge ICs

Aimed at industrial applications, a family of USB to serial bridge devices provides a straightforward way to interface with RS-232 or RS-485 serial networks through USB using a minimum of components and PCB space. The XR21B1420, XRB21B1422, and XRB21B1424 provide 1, 2, and 4 UART channels respectively. The XRB21B1421 provides a single



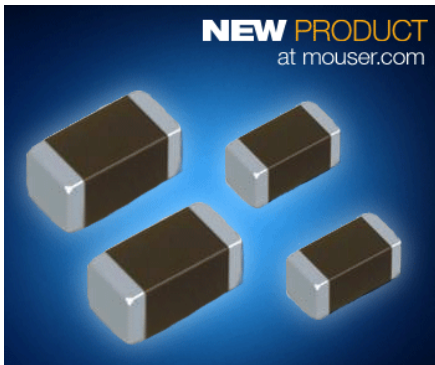
channel UART and uses the native operating system HID (Human Interface Device) driver. The XR21B142x devices are fully compliant to the USB 2.0 (Full-Speed) specification with 12 Mbps USB data transfer rate, and deliver significantly higher data throughput compared to competing devices, especially when multiple channels are operating simultaneously. Exar says the ubiquity of USB has left some serial-only connections "stranded" and you can use the HID profile as a simple, if lower-speed, means of bridging to them.

[Complete article, here](#)

MLCC caps to 330µF, now in distribution

Mouser now has Taiyo Yuden's large capacitance 330µF high end capacitor in an MLCC package, claimed to be the first of its kind. These small devices offer

a high capacitance, low equivalent series resistance (ESR), and low impedances at high frequencies. The capacitor occupies an EIA 1210 package. Taiyo Yuden



has expanded its capacitor product lines to include new capacitances in their EMK (16 VDC), AMK (4 VDC), TMK (25 VDC), and UMK (50 VDC) multilayer ceramic capacitor families. These new capacitors are available in packages as small as 0.4 x 0.2 mm, are built on a monolithic structure for increased reliability, and also offer wide range of capacitance values in standard case sizes. Very low impedance at high frequency makes for good noise decoupling performance.

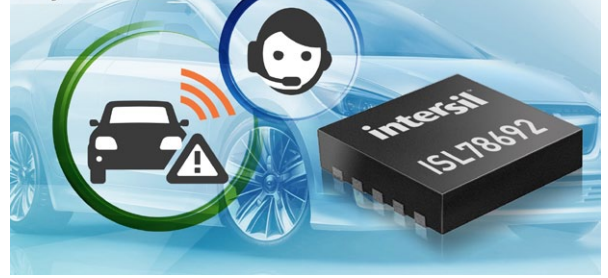
[Complete article, here](#)

Lithium-ion charger maintains vehicle eCall batteries

ISL78692 is a battery charger IC with very low leakage current; it is specifically designed to extend the life of an eCall (automatic emergency call system) backup battery when vehicle battery is off. The 4.1V charger has lower leakage current (3 µA) than alternative solutions, allowing the backup battery to remain charged for a longer period of time. Lower charging voltage also extends

battery life while the device's small footprint reduces total solution size. The ISL78692 charger's ability to monitor the battery's temperature and its low, 4.1V output voltage both help to extend the life of, specifically, LiFePO4 (lithium-iron-phosphate) batteries, which are commonly used in this function. Highly integrated, the ISL78692 requires five external components to program the charging current. The ISL78692 also offers a charge current thermal foldback feature that prevents overheating by automatically reducing the battery charging current.

ISL78692: Li-ion Single Cell Battery Charger for Emergency Call Safety Systems

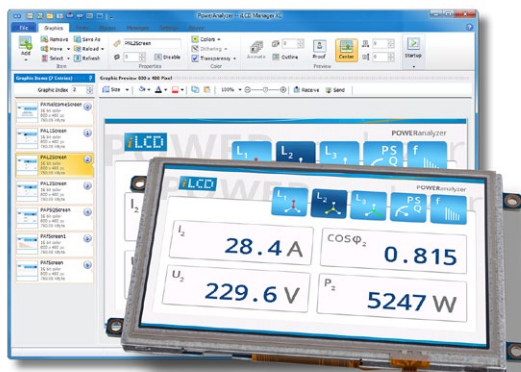


[Complete article, here](#)

Intelligent touch displays with high-level commands

Displays company demmel products (Vienna and Munich) has added intelligent touch displays in 4.3-, 5.7- and 7in. formats, all equipped with the fast DPC3090 controller and 128 MByte of flash memory. With the DPC3090 processor, execution times and

transmission rates increase by over 50% as compared to the earlier panels. All graphics, animations, fonts, text modules and macros used to design



the display can be stored on the 128 MByte flash memory, a 4x upgrade. The integrated iLCD controller includes more than 250 high-level commands to control the iLCDs via Ethernet, USB, RS232, I²C or SPI interfaces; formatting text output, drawing static and animated graphics, filling areas with predefined colour gradients or tiles, changing the transparency on arbitrary display areas or touch screen control.

[Complete article, here](#)

Controller manages 14-cell lithium ion sources to ASIL-C

Freescale's integrated battery cell controller is designed to improve functional safety, robustness and affordability; it balances measurement accuracy, scalability and high speed isolated communications for automotive and industrial battery management. The integrated 14-cell lithium-ion battery cell controller is aimed at industrial and automotive applications, designed to cost effectively meet the stringent requirements for ASIL-C functional safety. With 14 cell balancing transistors, a current sensor with ±0.5% accuracy from milliamps to kiloamps, and 2 Mbps communication transceiver interface integrated into a single 64-pin QFP package, the MC33771 battery cell controller and companion MC33664 isolated communications interface handle 48V battery systems, enabling economical scalability beyond 1000V. Built-in diagnostics help protect automotive and industrial battery packs against critical fault conditions, and its transformer-coupled isolated high speed transceiver eliminates the need for expensive isolated CAN buses to meet ASIL-C requirements. Embedded functional verification and fault diagnostics enable compliance with ISO 26262 ASIL-C functional safety standards without additional external circuitry. For higher voltage systems, the integrated daisy chain differential transceiver communicates at 2 Mbps using transformer coupled isolation up to 3750V, while the MC33664 connects the battery pack directly to the system MCU's dual SPI interface using the same transformer coupled isolation.

[Complete article, here](#)

Qt grows for mobile app and HMI development

Having, until now, grown the Qt line as a product under the Digia name, activity has risen to the level where Digia has formed "The Qt Company" as a wholly owned subsidiary, to drive future Qt development and market expansion. Under The Qt Company, a new Qt product site, www.qt.io is launched unifying the commercial business and open source community under one online channel. A €20 Indie Mobile monthly subscription plan is also added, targeting mobile app developers with a commercially-licensed flexible and affordable package for mobile app development and deployment to the most popular stores. Qt is noted for its "write-once/run anywhere" UI development approach.

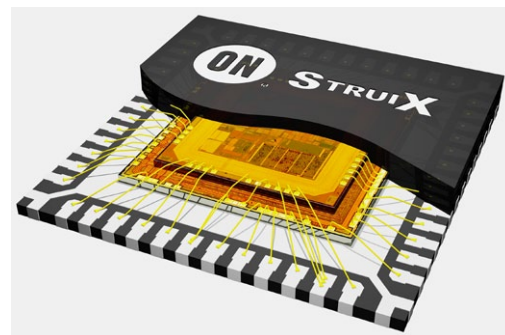


Qt is a C++ based framework of libraries and tools that enables the development of powerful, interactive and cross-platform applications and devices. Qt's support for multiple desktop, embedded and mobile operating systems allows developers to save time related to application and device development by reusing one code.

[Complete article, here](#)

ARM-based, SiP for precision medical sensing

A semi-customisable, power efficient system-in-package (SiP) solution enables miniature sensing systems for mHealth applications including glucose monitors, heart rate monitors, and electrocardiogram analysers. ON Semiconductor created the Struix stacked-dice, system-in-package format to meet product development demands in the portable medical market; the semi-customisable SiP is aimed at precision sensing and monitoring in



a variety of mobile medical electronics including glucose monitors, heart rate monitors and electrocardiogram analysers. Struix ("stacked")

uses advanced die-on-die technology to integrate a custom-designed analogue front-end (AFE) on top of an 32-bit ASSP microcontroller (ULPMC10), to form a complete miniature system. The ULPMC10 microcontroller element of Struix processes signals using a 32-bit ARM Cortex-M3 core running up to frequencies of 30 MHz.

[Complete article, here](#)

Ultra-low power conversion for wearables & sensors

Texas Instruments claims to have the industry's smallest and lowest-power battery charger, for use with ultra-low-power designs, such as wearables and remote sensor nodes; this introduction comprises a



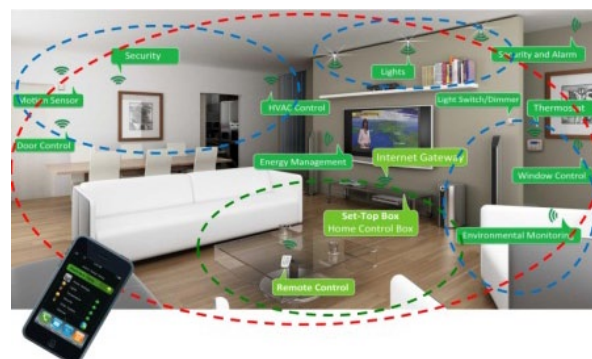
very small and low power linear battery charger and a tiny, fully integrated DC/DC power module, which consumes only 360 nA of quiescent current, to help extend battery run-time in wearable electronics, remote sensors

and MSP430 microcontroller-based applications. The bq25100 single-cell Li-Ion charger comes in a 0.9 x 1.6-mm WCSP package, and achieves a solution half the size of existing charger solutions. The device supports input voltages up to 30V, and allows accurate control of fast-charge currents as low as 10 mA or as high as 250 mA, and precise charge termination down to 1 mA, to support tiny Li-Ion coin batteries. The bq25100 also has a leakage current of less than 75 nA to extend standby operation.

[Complete article, here](#)

Remote control IC with voice control functions

GreenPeak Technologies' GP565 Smart Home radio chip for remote controls supports voice control, motion sensing and the ZRC 2.0 protocol. It is aimed at "next generation" remotes using RF instead of infrared (IR), to build a single remote for all Smart Home systems. The new ZigBee ZRC 2.0 protocol enables a single remote control to control



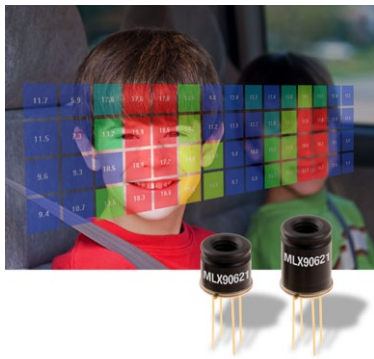
all the home's connected devices – including turning on lights, opening curtains, managing appliances and environment. The 'IR-RF Download' feature

provides complete control of legacy audio and video equipment, either through RF4CE or infrared, with a hybrid remote control, without requiring the user to select the correct IR settings for the TV. ZRC 2.0 is fully backward compatible with existing ZRC 1.x implementations. The voice control features enables users to control the remote without having to navigate a confusing nest of buttons. GreenPeak uses a reliable compression codec to enhance throughput within the available ZigBee data rate and advanced voice recognition.

[Complete article, here](#)

Infrared sensor array sees a wider field

Low cost infra-red (IR) arrays provide precise imaging data and detailed heat signatures for both static and dynamic objects and find applications in security, automotive,



building automation and consumer electronics. With a 16 x 4 pixel configuration, the MLX90621 from Melexis can offer a field of view (FoV) of 100° x 25° - significantly greater than the company's previous generation of IR array products. It also has 4-times faster measurement speeds, equating

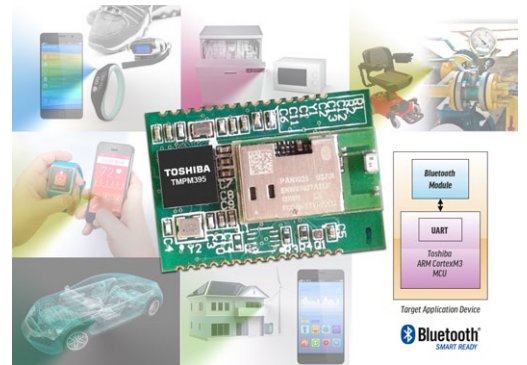
to a dramatic reduction in the inherent noise levels present. Factory calibrated to operate over a temperature range of -40°C to 85°C, this array can accurately measure object temperatures from -20°C to 300°C. Interface and control is managed via the device's I²C digital interface. The speed is programmable, with a frame rate covering 0.5 Hz to 64 Hz supported. Noise vs. speed performance is characterised by 0.25K noise equivalent temperature difference (NETD) at a frequency of 16 Hz.

Complete article, here



Drop-in Bluetooth 4.0 module-on-module for control systems

Toshiba has a development module-on-module (or "Module2") that combines a Bluetooth 4.0 module with a microcontroller in order to shorten development times. The Module2 enables simple integration into sensor control systems, lighting and heating systems, PC peripheral systems and legacy host control systems. The Module2 measures 25 x 17 mm and is suited for battery driven applications. It comprises a



Toshiba TMPM395FWAXBG ARM Cortex M3 core MCU along with a Panasonic PAN1026 Bluetooth 4.0 dual mode module, with antenna, that incorporates a Toshiba TC35661-501 Bluetooth LSI with embedded Bluetooth stack and SPP and BLE Gatt profiles. The Bluetooth module is programmable using high-level Bluetooth APIs and includes 128 kB NAND flash memory to store the Bluetooth host control and system application software. The device supports a range of hardware interfaces including UART, I²C, SPI and JTAG debugger interface.

Complete article, here



FRAM MCUs for metering, health/fitness and wearables

Texas Instruments has added to its ferroelectric-RAM MCUs with the ultra-low-power MSP430FR69x that has integrated smart analogue, extended scan interface, LCD controller and up to 128 kB memory. Reducing power consumption, bill of materials and product size, TI has 46 new

ultra-low-power MSP430 FRAM microcontrollers (MCUs) with more memory, features and integration. These MCUs are scalable up to 128 kB non-volatile FRAM memory and include smart analogue integration, such as an extended scan interface

(ESI) and a differential input analogue-to-digital converter (ADC) that consumes as little as 140 µA at 200 ksamples/sec. Developers can also use the integrated 320-segment LCD controller to add a display to their products and a 256-bit advanced encryption standard (AES) hardware accelerator to increase security of data transmissions.

Complete article, here



6-axis accelerometer/gyroscope uses "always on" power

From ST, this 6-axis inertial combination MEMS sensor (3A+3G) typically consumes 0.8 mA at 100 Hz, claimed to be at least 20% better than competition and 3-times lower than the current ST generation. The power-efficient, low-noise device is suited to Internet of Things, wearable, indoor navigation, and handheld applications, ST says, with performance figures including 0.6 mg RMS noise at ODR = 104 Hz, and typical gyro noise density of 7 mdps/√Hz at 10 Hz. The device has the largest-available data buffering, with time stamp, at 8 kBytes. This is the first iNEMO Ultra product - an always-on, high-performance 6-axis combination accelerometer and gyroscope that sets new standards for device and system power efficiency, signal noise, and performance in motion sensors. Together with ultra-low-power STM32 microcontrollers, the LSM6DS3 combos will create new possibilities for the development of battery-powered smart sensor systems to be embedded in mobile and wearable devices and innovative objects for the Internet of Things (IoT). The LSM6DS3 will be delivered as an optimised 2-chip system-in-package featuring high-performance 3-axis digital accelerometer and 3-axis digital gyroscope with integrated power-efficient modes down to 0.6 mA in always-on working mode.

Complete article, here



When in doubt, read the operator's manual

I am an electrical engineer for the manufacturing department of a defence company, and we build a gadget for our military that was originally designed by another company. One day there was a problem with the CPU card of the gadget and I was asked to look into it.

The problem was the CPU card's microprocessor wouldn't run. The test technicians said they turned on the gadget but it didn't boot up and operate. They actually had another gadget doing the same thing. I thought, "Uh oh, a trend." The CPU card used a ubiquitous microprocessor. The funny thing is that we built dozens of these gadgets with no problem but all of a sudden we had two in a row that didn't work.

I checked the usual things on the CPU card and made sure the microprocessor was getting power, was getting its clock, and was not in a reset state. The next thing to check was the address strobe. Ah, no activity. This could mean an open in an address or data line between the chip and the flash memory. So I started checking continuity. Hmm, no opens or shorts. Our in-circuit tester also confirmed that. There could be something wrong with the code in the flash. I had our repair people replace the flash chip and reprogram it. Still didn't work.

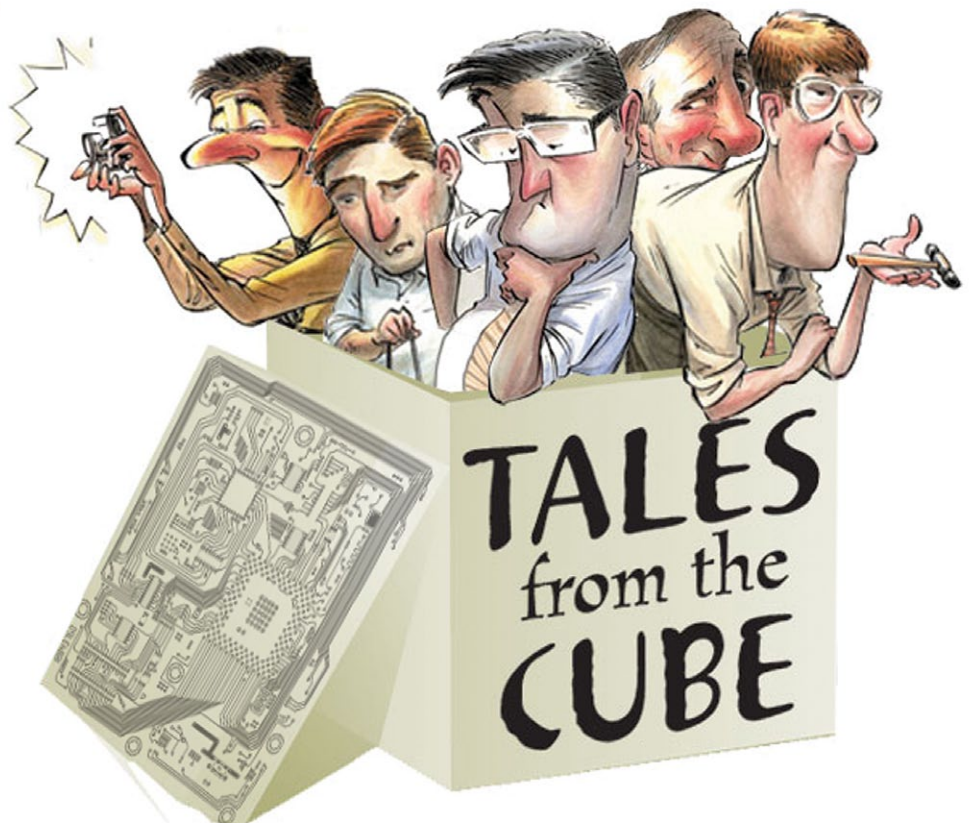
Then I decided to play around with the power-on reset circuit, just for kicks. When power is applied, there is a little RC circuit to keep it in reset for half a second while the power supply lines stabilise before releasing the reset so it will boot up. The circuit was working fine but I decided to add more capacitance to the RC circuit and lengthen the power-on reset time to about 2 seconds. Voila, the processor started working. Well, that's good: but weird. Why would lengthening the reset time make it start working?

I went and looked at the other CPU card that wasn't booting up and I did the same thing to its power-on reset and lengthened the RC time constant to 2 seconds. No dice; it didn't work. I then lengthened the RC time to 13 seconds, and the processor started working. Wow, that was strange. I realised I was seeing symptoms but not the true problem. I put everything back to the original. Now I decided I better get the micro-

processor operator's manual and start reading. That's when I found the answer to my problem.

The microprocessor operator's manu-

an indeterminate state and not work. Most of the time it worked, but on a few CPU cards it didn't work. The bad thing about this race condition is that it may work today, but there's no guarantee



al had a warning paragraph buried in the middle of the book plainly stating not to do what the original designers were accidentally doing. It said; do not apply the system clock to the microprocessor while the microprocessor is being powered up. The original designers violated the manufacturer's caveat.

The circuit of our CPU card is such that the clock chip and the processor are being powered from the same 5V line and thus the processor is getting a clock signal applied while it is being powered up. According to the processor manufacturer, that's a no-no. What's actually happening with this setup is that there is a race condition between the clock application and the processor power-up. If the clock got to the processor before it was fully powered up, the processor could come up into

it will work tomorrow. We had a bunch of these gadgets in the field with a non-100% guarantee they'll work every single solitary time.

The fix was simple in our application. The clock chip on the CPU card was of the type that had a tri-state control that was normally pulled up with a 10K resistor. All we had to do was add a 10 μ F capacitor to ground to form an RC time delay. This way the clock output didn't appear until about 30 msec after the power was applied, which was enough time for the processor to power up and run without hanging. It fixed the problem. We then retrofitted all the units in the field. We haven't had a problem since. Case closed.

Mike Kornacker has been an electrical engineer in the defence industry for 34 years.